Chapter # 4: Programmable and Steering Logic

Contemporary Logic Design
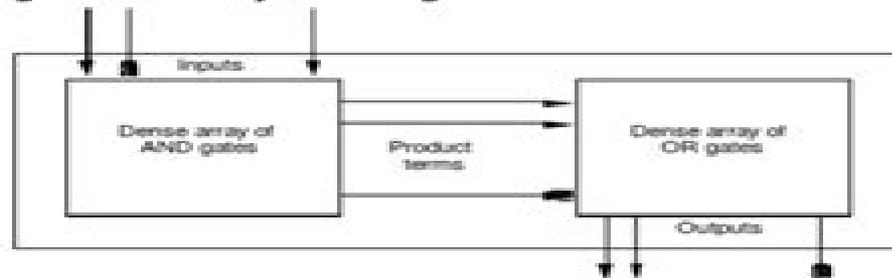
Randy H. Katz
University of California, Berkeley

June 1993

PALs and PLAs

Pre-fabricated building block of many AND/OR gates (or NOR, NAND) "Personalized" by making or breaking connections among the gates

Programmable Array Block Diagram for Sum of Products Form

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Stamatis Vassiliadis,Dimitrios Soudris

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Tools and Algorithms for the Construction and Analysis of Systems Bernhard Steffen,1998-03-18 ETAPS 99 is the second instance of the European Joint Conferences on Theory and Practice of Software ETAPS is an annual federated conference that was established in 1998 by combining a number of existing and new conferences This year it comprises ve conferences FOSSACS FASE ESOP CC TACAS four satellite workshops CMCS AS WAGA CoFI seven invited lectures two invited tutorials and six contributed tutorials The events that comprise ETAPS address various aspects of the system velopment process including speci cation design implementation analysis and improvement The languages methodologies and tools which support these tivities are all well within its scope Dieren t blends of theory and practice are represented with an inclination towards theory with a practical motivation on one hand and soundly based practice on the other Many of the issues involved in software design apply to systems in general including hardware systems and the emphasis on software is not intended to be exclusive *Asynchronous Circuit Design for VLSI Signal Processing* Teresa H. Meng,Sharad Malik,2011-06-27 Asynchronous Circuit Design for VLSI Signal Processing is a collection of research papers on recent advances in the area of specification design and analysis of asynchronous circuits and systems This interest in designing digital computing systems without a global clock is prompted by the ever growing difficulty in adopting global synchronization as the only efficient means to system timing Asynchronous circuits and systems have long held interest for circuit designers and researchers alike because of the inherent challenge involved in designing these circuits as well as developing design techniques for them The frontier research in this area can be traced back to Huffman s publications The Synthesis of Sequential Switching Circuits in 1954 followed by Unger s book Asynchronous Sequential Switching Circuits in 1969 where a theoretical foundation for handling logic hazards was established In the last few years a growing number of researchers have joined force in unveiling the mystery of designing correct asynchronous circuits and better yet have produced several alternatives in automatic synthesis and verification of such circuits This collection of research papers represents a balanced view of current research efforts in the design synthesis and verification of asynchronous systems Cross-Talk Noise Immune VLSI Design Using Regular Layout Fabrics Robert K. Brayton,Alberto L. Sangiovanni-Vincentelli,2012-12-06 This book was motivated by the problems being faced with shrinking IC process feature sizes It is well known that as process feature sizes shrink a host of electrical problems like cross talk electromigration self heat etc are becoming important Cross talk is one of the major problems since it results in unpredictable design behavior In particular it can result in significant delay variation or signal integrity problems in a wire depending on the state of its neighboring wires Typical approaches to tackle the cross talk problem attempt to fix the problem once it is created In our approach we ensure that cross talk is eliminated by design The work described in this book attempts to take an outside the box view and propose a radically different design style This design style first imposes a fixed layout pattern or fabric on the integrated circuit and then embeds the circuit being

implemented into this fabric The fabric is chosen carefully in order to eliminate the cross talk problem being faced in modem IC processes With our choice of fabric cross talk between adjacent wires on an IC is reduced by between one and two orders of magnitude In this way the fabric concept eliminates cross talk up front and by design We propose two separate design flows each of which uses the fabric concept to implement logic The first flow uses fabric compliant standard cells as an implementation vehicle We call these cells fabric cells and they have the same logic functionality as existing standard cells with which they are compared   <u>Field-programmable Logic and Applications</u> ,1992   *Reconfigurable Computing* Scott Hauck,André DeHon,2010-07-26 Reconfigurable Computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design the key feature of reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution Reconfigurable computers serve as affordable fast and accurate tools for developing designs ranging from single chip architectures to multi chip and embedded systems Scott Hauck and Andre DeHon have assembled a group of the key experts in the fields of both hardware and software computing to provide an introduction to the entire range of issues relating to reconfigurable computing FPGAs field programmable gate arrays act as the computing vehicles to implement this powerful technology Readers will be guided into adopting a completely new way of handling existing design concerns and be able to make use of the vast opportunities possible with reconfigurable logic in this rapidly evolving field Designed for both hardware and software programmers Views of reconfigurable programming beyond standard programming languages Broad set of case studies demonstrating how to use FPGAs in novel and efficient ways   *Proceedings of the 1984 Custom Integrated Circuits Conference, Genesee Plaza/Holiday Inn, Rochester, NY, May 21-23, 1984* ,1984   **Fine- and Coarse-Grain Reconfigurable Computing** Stamatis Vassiliadis,Dimitrios Soudris,2007-10-12 Fine and Coarse Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine or FPGA and Coarse Grain Reconfigurable Architectures Recently developed integrated architecture design and software supported design flow of FPGA and coarse grain reconfigurable architecture are also described Part I consists of two extensive surveys of FPGA and Coarse Grain Reconfigurable Architectures The FPGA technology is defined which includes architecture logic block structure interconnect and configuration methods and existing fine grain reconfigurable architectures emerged from both academia and industry Additionally the implementation techniques and CAD tools developed to facilitate the implementation of a system in reconfigurable hardware by the industry and academia are provided In addition the features the advantages and limitations of the coarse grain reconfigurable systems the specific issues that should be addressed during the design phase as well as representative existing coarse grain reconfigurable systems are explained In Part II case studies innovative research results about reconfigurable architectures and design frameworks from three projects AMDREL MOLEN and ADRES DRESC and a new classification according to microcoded architectural criteria are described Fine and Coarse Grain Reconfigurable

Computing is an essential reference for researchers and professionals and can be used as a textbook by undergraduate graduate students and professors Foreword by Yale Patt Jim Smith and Mateo Valero *Tools and Algorithms for the Construction and Analysis of Systems* ,1998 *Introduction to Electronics Design* Ferdinand Haverman Mitchell (Jr.),Ferdinand Haverman Mitchell,1992 **Comprehensive Dissertation Index** ,1989 **VLSI Design Techniques for Analog and Digital Circuits** Randall L. Geiger,Phillip E. Allen,Noel R. Strader,1990 **VLSI Fault Modeling and Testing Techniques** George W. Zobrist,1993 VLSI systems are becoming very complex and difficult to test Traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated ciruit Hierarchial models are needed that are easy to use at the transistor and functional levels Stuck open faults present severe testing problems in CMOS circuits to overcome testing problems testable designs are utilized Bridging faults are important due to the shrinking geometry of ICs BIST PLA schemes have common features controllability and observability which are enhanced through additional logic and test points Certain circuit topologies are more easily testable than others The amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty Test implementation is usually left until after the VLSI data path has been synthesized into a structural description This leads to investigation methodologies for performing design synthesis with test incorporation These topics and more are discussed **Advances in Computers** Marvin Zelkowitz,2002-09-06 Advances in Computers remains at the forefront in presenting the new developments in the ever changing field of information technology Since 1960 Advances in Computers has chronicled the constantly shifting theories and methods of this technology that greatly shape our lives today Volume 56 presents eight chapters that describe how the software hardware and applications of computers are changing the use of computers during the early part of the 21st century Software Evolution and the Staged Model of the Software Lifecycle Embedded Software Empirical Studies of Quality Models in Object Oriented Systems Software Fault Prevention by Language Choice Quantum computing and communication Exception Handling Breaking the Robustness Barrier Recent Progress on the Design of Robust Multimodal Systems Using Data Mining to Discover the Preferences of Computer Criminals As the longest running continuous serial on computers Advances in Computers presents technologies that will affect the industry in the years to come covering hot topics from fundamentals to applications Additionally readers benefit from contributions of both academic and industry professionals of the highest caliber Software Evolution and the Staged Model of the Software Lifecycle Embedded Software Empirical Studies of Quality Models in Object Oriented Systems Software Fault Prevention by Language Choice Quantum computing and communication Exception Handling Breaking the Robustness Barrier Recent Progress on the Design of Robust Multimodal Systems Using Data Mining to Discover the Preferences of Computer Criminals **Driving Scientific and Engineering Discoveries Through the Integration of Experiment, Big Data, and Modeling and Simulation** Jeffrey Nichols,Arthur 'Barney' Maccabe,James Nutaro,Swaroop Pophale,Pravallika Devineni,Theresa

Ahearn,Becky Verastegui,2022-03-09 This book constitutes the revised selected papers of the 21st Smoky Mountains Computational Sciences and Engineering Conference SMC 2021 held in Oak Ridge TN USA in October 2021 The 33 full papers and 3 short papers presented were carefully reviewed and selected from a total of 88 submissions The papers are organized in topical sections of computational applications converged HPC and artificial intelligence advanced computing applications use cases that combine multiple aspects of data and modeling advanced computing systems and software connecting instruments from edge to supercomputers deploying advanced computing platforms on the road to a converged ecosystem scientific data challenges The conference was held virtually due to the COVID 19 pandemic *Equational Programming* Nachum Dershowitz,David A. Plaisted,1986 **1992 IEEE International Symposium on Circuits and Systems** Stanley A. White,Institute of Electrical and Electronics Engineers,1992 ISCAS 98 provides the latest results on many important subjects in computer aided design modeling and simulation testing signal processing neural and fuzzy systems multimedia image and video processing linear and nonlinear circuits and systems and many more exciting fields *Proceedings* ,1983 **Data Processing Annual** ,1961 **Dissertation Abstracts International** ,1989 *IEEE, ACM International Conference on Computer Aided Design* International Conference on Computer Aided Design. Institute of Electrical and Electronics Engineers, 2000, San José, Calif..,2000

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