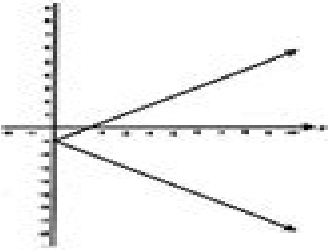


Unit 1 Day 03 – Review of Functions, Function Notation, and Characteristics

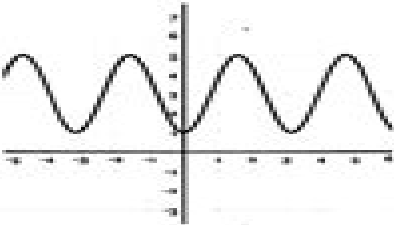
Determine whether each of the following is a function. Explain using the definition of a function.

1.



This graph is not a function because it fails the vertical line test.

2.



This graph is a function because it passes the vertical line test.

3.

x	y
0	14
1	11
2	7
3	6
3	5
4	3
5	2
6	1

This table is not a function because 3 has two outputs

Evaluate each of the following.

4. Given $f(x) = x - 6$,
Find $f(3)$.

$$3 - 6 = \textcircled{-3}$$

5. Given $f(x) = -x^2 - 6x - 6$,
Find $f(-2)$.

$$-(-2)^2 - 6(-2) - 6 = \textcircled{10}$$

6. Given $-3|x + 3| + 7$,
Find $f(-7)$.

$$-3|-7 + 3| + 7 = -3(4) + 7 = \textcircled{-5}$$

7. Given the table

x	g(x)
-5	-10
6	3
-6	4
-1	3

Find the following:

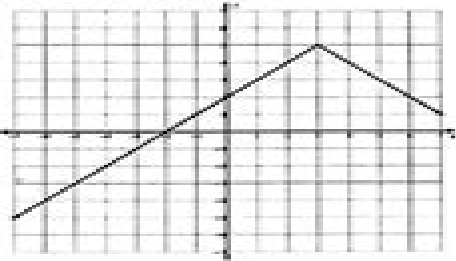
$$g(-5) = -10$$

$$g(-1) = 3$$

When $g(x) = 4, x = ?$ -6

When $g(x) = 3, x = ?$ 6 and -1

8. Given the graph



Find the following:

$$f(-4) = -2$$

$$f(5) = 3$$

When $f(x) = 4, x = ?$ 2

When $f(x) = -1, x = ?$ -3

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James J. Rizzuto



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web as an alternative you can also write your simulation stimulus using generic vhdl code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libraries that are supported by almost all vhdl compilers specific silicon

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web for sample syntax and a list of vhdl statements supported by the vhdl synthesizer see appendix a quick reference for a list of exceptions and constraints on the vhdl synthesizer s support of vhdl see appendix b limitations this chapter shows you the structure of a vhdl design and then

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web nov 8 2018 in this post we will take a look at implementing the vhdl code for all logic gates using dataflow architecture first we will take a look at the logic equations of all the gates and then the syntax we will also test our logic by writing a testbench

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web from wikipedia the free encyclopedia [vhdl source for a signed vhsic hardware description languagevhdl is a hardware description language hdl that can model the behavior and structure of at multiple levels of abstraction ranging from the system level down to that of logic gates for design entry documentation and verification purposes](#)

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web [vhdl tool vhdl tool provides a language server for the vhdl hardware description language this plugin makes vhdl tool s language server interface available from within vscode this is beta quality code report bugs here](#)

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web apr 7 2014 the vhdl code for full adder circuit adds three one bit binary numbers a b cin and outputs two one bit binary

numbers a sum s and a carry cout truth table describes the functionality of full adder sum s output is high when odd number of inputs are high cout is high when two or more inputs are high

[and all elements of an n bit array in vhdl stack overflow](#) - Apr 14 2022

web nov 30 2013 lets say i have an n bit array i want to and all elements in the array similar to wiring each element to an n bit and gate how do i achieve this in vhdl note i am trying to use reusable vhdl code so i want to avoid hard coding

something like result array 0 and array 1 and array 2 and array n thanks oshara

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web this tutorial describes language features that are common to all versions of the language they are expressed using the syntax of vhdl 93 and subsequent versions there are some aspects of syntax that are incompatible with the original vhdl 87 version however most tools now support at least vhdl 93 so syntactic differences

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web feb 16 2023 by using the coding style above there is no question about which version of bottom is wanted the version in the library my lib1 is the correct one care should be taken when choosing library names for vhdl files while a library called work is a common library name for many projects the tool will handle it a little differently than

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web high level synthesizable vhdl hvhdl is a set of coding patterns for standard vhdl which are designed to greatly increase abstraction level of vhdl source code using standard synthesis tools the coding patterns are designed to support incremental design testing and development of the vhdl source code

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web overview visual studio code is an open source editor from microsoft vhdl tool makes its services available to vs code through the language server protocol vscode plugin find the plugin by searching for vhdl in the extensions sidebar or go to the online marketplace follow the instructions in the readme

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web dec 29 2017 vhdl uses a similar description however it has its own syntax for example it uses the following lines of code to describe the input and output ports of this circuit 1 entity circuit 1 is 2 port a in std logic 3 b in std logic 4 out1 out std logic 5 end circuit 1

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web apr 29 2016 vhdl was created in the 1980s to develop a high speed integrated circuit it has since become an industry standard language for describing digital systems at the structural or behavioral levels in a text based format the vhdl file can be used to manufacture a physical circuit such as a motherboard processor or memory module

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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web quartus and vhdl code in this section you should learn how to implement a vhdl code for single cycle data path before we go any further let s define some of the terms that we use throughout the book entity all designs are expressed in terms of entities an entity is the most basic building block in a design