

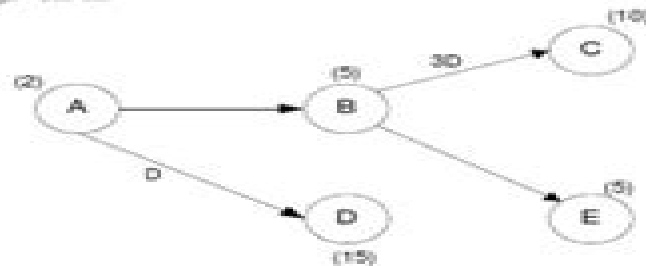
## Solutions to Assignment #4 Chapter 5

5. The critical path lengths of an unfolded DFG only increase when a new arc is generated with no delays in the DFG; otherwise the path lengths remain the same. An arc with  $D$  delays in the original DFG produces  $J-D$  arcs with no delays in the  $J$ -unfolded DFG when  $J > D$ .

If  $J > D$ , then the  $J$  unfolded graph will contain an additional arc without delays, and the path length for the  $J$ -unfolded DFG increases through those nodes, compared to the  $(J-1)$  unfolded DFG.

Therefore, the critical path of the  $J$ -unfolded graph is greater than or equal to that of the  $(J-1)$  unfolded graph.

7. The DFG is given as



The computation for the critical path  $A \rightarrow B \rightarrow E$  is given as  $12 \text{ u.t.} = T_{crit}^0$ .

Following the algorithm given in Problem 6, we have:

$$T_{crit}^0 = 2 + 5 + 5 = 12;$$

$$J' = \left\lceil \frac{12}{8} \right\rceil = 2$$

Applying unfolding of degree 2 we get

# Parhi Solution Unfolding

**Tobias Bleicker**



## **Parhi Solution Unfolding:**

**Principles and Practice of Constraint Programming -- CP 2011** Jimmy Lee, 2011-09-01 This book constitutes the refereed proceedings of the 17th International Conference on Principles and Practice of Constraint Programming CP 2011 held in Perugia Italy September 12 16 2011 The 51 revised full papers and 7 short papers presented together with three invited talks were carefully reviewed and selected from 159 submissions The papers are organized in topical sections on algorithms environments languages models and systems applications such as decision making resource allocation and agreement technologies

**Pipelined Lattice and Wave Digital Recursive Filters** Jin-Gyun Chung, Keshab K. Parhi, 2012-12-06 Pipelined Lattice and Wave Digital Recursive Filters uses look ahead transformation and constrained filter design approaches It is also shown that pipelining often reduces the roundoff noise in a digital filter The pipelined recursive lattice and wave digital filters presented are well suited where increasing speed and reducing area or power or roundoff noise are important Examples are wireless and cellular codec applications where low power consumption is important and radar and video applications where higher speed is important The book presents pipelining of direct form recursive digital filters and demonstrates the usefulness of these topologies in high speed and low power applications It then discusses fundamentals of scaling in the design of lattice and wave digital filters Approaches to designing four different types of lattice digital filters are discussed including basic one multiplier normalized and scaled normalized structures The roundoff noise in these lattice filters is also studied The book then presents approaches to the design of pipelined lattice digital filters for the same four types of structures followed by pipelining of orthogonal double rotation digital filters which eliminate limit cycle problems A discussion of pipelining of lattice wave digital filters follows showing how linear phase narrow band sharp transition recursive filters can be implemented using this structure This example is motivated by a difficult filter design problem in a wireless codec application Finally pipelining of ladder wave digital filters is discussed Pipelined Lattice and Wave Digital Recursive Filters serves as an excellent reference and may be used as a text for advanced courses on the subject

**Accelerator Data-Path Synthesis for High-Throughput Signal Processing Applications** Werner Geurts, Francky Catthoor, Serge Vernalde, Hugo De Man, 2011-06-27 Accelerator Data Path Synthesis for High Throughput Signal Processing Applications is the first book to show how to use high level synthesis techniques to cope with the stringent timing requirements of complex high throughput real time signal and data processing The book describes the state of the art in architectural synthesis for complex high throughput real time processing Unlike many other the Synthesis approach used in this book targets an architecture style or an application domain This approach is thus heavily application driven and this is illustrated in the book by several realistic demonstration examples used throughout Accelerator Data Path Synthesis for High Throughput Signal Processing Applications focuses on domains where application specific high speed solutions are attractive such as significant parts of audio telecom instrumentation speech robotics medical and automotive processing image and

video processing TV multi media radar sonar etc Moreover it addresses mainly the steps above the traditional scheduling and allocation tasks which focus on scalar operations and data Accelerator Data Path Synthesis for High Throughput Signal Processing Applications is of interest to researchers senior design engineers and CAD managers both in academia and industry It provides an excellent overview of what capabilities to expect from future practical design tools and includes an extensive bibliography

**Embedded and Ubiquitous Computing** Edwin Sha,Sung-Kook Han,Cheng-Zhong Xu,Moon Hae Kim,Laurence T. Yang,Bin Xiao,2006-10-06 This book constitutes the refereed proceedings of the International Conference on Embedded and Ubiquitous Computing EUC 2006 held in Seoul Korea August 2006 The book presents 113 revised full papers together with 3 keynote articles organized in topical sections on power aware computing security and fault tolerance agent and distributed computing wireless communications real time systems embedded systems multimedia and data management mobile computing network protocols middleware and P2P and more

**High-Performance VLSI Signal Processing Innovative Architectures and Algorithms, Algorithms and Architectures** K. J. Ray Liu,Kung Yao,1998 Electrical Engineering Signal Processing High Performance VLSI Signal Processing Innovative Architectures and Algorithms Volume 1 Algorithms and Architectures The first volume in a two volume set High Performance VLSI Signal Processing Innovative Architectures and Algorithms brings together the most innovative papers in the field focused introductory material and extensive references The editors present timely coverage of algorithm and design methodologies with an emphasis on today s rapidly evolving high speed architectures for VLSI implementations These volumes will serve as vital resources for engineers who want a comprehensive knowledge of the extremely interdisciplinary field of high performance VLSI processing The editors provide a practical understanding of the merits of total system design through an insightful synergistic presentation of methodology architecture and infrastructure Each volume features Major papers that span the wide range of research areas in the field Chapter introductions including historical perspectives Numerous applications oriented design examples Coverage of current and future technological trends Thorough treatment of high speed architectures

**Recent Advancements in Product Design and Manufacturing Systems** B B V L Deepak,M.V.A. Raju Bahubalendruni,D.R.K. Parhi,B. B. Biswal,2024-11-16 This book presents select proceedings of the 5th Innovative Product Design and Intelligent Manufacturing System IPDIMS 2023 conference It covers concepts and recent methods that are implemented in intelligent manufacturing systems along with the product innovation technologies The broad topics covered include Industry 4 0 Industry 5 0 smart manufacturing advanced robotics product innovation and CAD CAM CIM The contents of this book are useful for academics as well as professionals working in the areas of mechatronics mechanical manufacturing production and industrial engineering

**ICASSP 91** ,1991 Proceedings of the National Science Council, Republic of China ,1999

**First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis** ,2003

**IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis** ,2003

**Performance-driven Partitioning Using Retiming and Replication** Lung-Tien Liu,1994 *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology* ,2007 VLSI Signal Processing, VIII IEEE Signal Processing Society,1995 **Proceedings of the 11th International Symposium on System Synthesis** ,1998 This is a collection of papers presented at the 11th International Symposium on System Synthesis It covers topics such as code generation optimization issues application specific synthesis techniques synchronization and interface issues instruction encoding and software synthesis techniques **Performance-driven System Partitioning** Lung-Tien Liu,1993 **TAO** Shan-Hsi Huang,1997 **VLSI Signal Processing, IX** IEEE Signal Processing Society,1996 VLSI signal processing components of portable systems in communications are described System equipment and component designs for low power and small size critical to product success are described Applications to the wireless network and cellular communications are given Computers and Their Applications Narayan C. Debnath,1998 *Fifth International Conference on High Performance Computing : Proceedings* IEEE Computer Society. Technical Committee on Parallel Processing,1998 Partial Contents Architecture Algorithms Compilers Communication System Software Interconnection Networks Scheduling Databases Distributed Systems Applications **Mathematical Reviews** ,2006

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