

# Computer Architecture 1 Final Exam

ELE319, Hanyang University, 2019 Spring.  
ID: \_\_\_\_\_ Name: \_\_\_\_\_

Department: \_\_\_\_\_

The first two problems are mandatory. If you fail to answer the questions, you will not receive any credit.

- (5pt) Specify the 5-stage pipeline and explain what operation is performed at each stage.
- (5pt) Specify three hazards in processor pipelining and explain hardware and software approaches to solve the hazards.
- (5pt) Write the output value (C) for the given circuits if  $A=1$  and  $B=1$ .



- (5pt) We construct a 2-bit multiplier using Mux as following. Two inputs are provided to a selector in Mux. For instance,  $01 * 01 = 0001$  and  $00 * 00 = 0000$  in the following figure. Fill the remained constant input values in the Mux to complete the multiplier. (1.5pt)



- (5pt) Similarly, we are constructing a divider using a ROM as following. In the example, if dividend is 5 and divisor is 2 then quotient is 2 and remainder is 1. Hence,  $0x21$  is stored at address  $0x52$ . What value should be stored at address  $0x53$  in the ROM to support the divider? (1.5pt)



- (5pt) What is the difference between latch and flip-flop? (5pt)
- (5pt) For the following arithmetic unit, we want to compute  $A-B$  where 2's complement number is used. Determine proper values for  $S1, S0, Cin$  to make  $F = A-B$ .



- (24pt) The following figure shows single cycle implementation for datapath and control path for MIPS architecture.



Fill 0, 1 or X(don't care) in the following table to implement for the architecture.

Instruction	ALU Op	MEMRs of Reg	Reg Write	Mem Read	Mem Write	Branch
R-type instruction	(1)	(2)	(3)	(4)	(5)	(6)
Load	(7)	(8)	(9)	(10)	(11)	(12)
Store	(13)	(14)	(15)	(16)	(17)	(18)
branch0	(19)	(20)	(21)	(22)	(23)	(24)

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**CL Gary**



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Mittermeir,2013-02-26 This book constitutes the refereed proceedings of the 6th International Conference on Informatics in Schools Situation Evolution and Perspectives ISSEP 2013 held in Oldenburg Germany in February March 2013 The 15 full papers included in this volume were carefully reviewed and selected from 48 submissions in addition the book contains two keynote talks in full paper length The contributions are organized in topical sections named from computer usage to computational thinking algorithmic and computational thinking games informatics in the context of other disciplines and competence based learning and retention of competencies **Progressive Architecture** ,1990 □□□□□□□□□□/□□□□ John L. Hennessy,□□□,David A. Patterson,1999

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