

Core Overview

The UART core with Avalon® interface implements a method to communicate serial character streams between an embedded system on an Altera® FPGA and an external device. The core implements the RS-232 protocol timing, and provides adjustable baud rate, parity, stop, and data bits, and optional RTS/CTS flow control signals. The feature set is configurable, allowing designers to implement just the necessary functionality for a given system.

The core provides an Avalon Memory-Mapped (Avalon-MM) slave interface that allows Avalon-MM master peripherals (such as a Nios® II processor) to communicate with the core simply by reading and writing control and data registers.

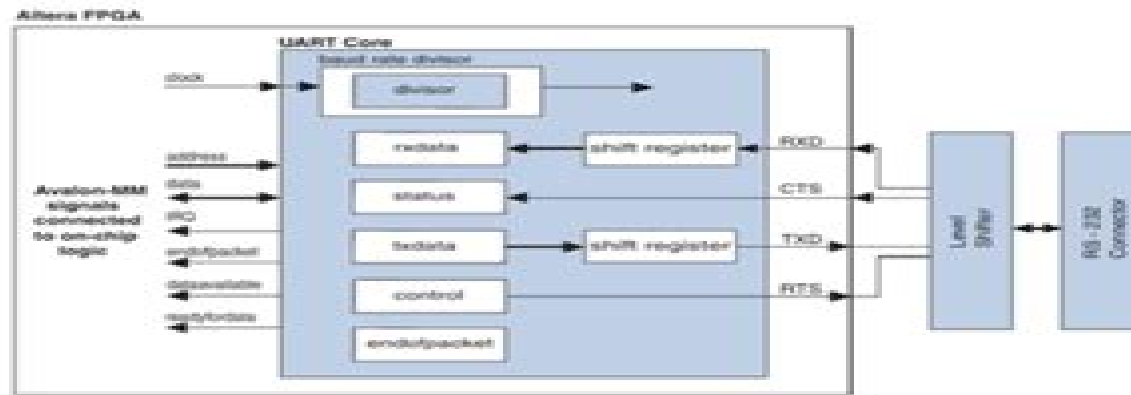
The UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. This chapter contains the following sections:

- "Functional Description"
- "Device Support" on page 6-3
- "Instantiating the Core in SOPC Builder" on page 6-3
- "Simulation Considerations" on page 6-7
- "Software Programming Model" on page 6-8

Functional Description

Figure 6-1 shows a block diagram of the UART core.

Figure 6-1. Block Diagram of the UART Core in a Typical System



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Table of Contents 6 Uart Core Altera

1. Understanding the eBook 6 Uart Core Altera
 - The Rise of Digital Reading 6 Uart Core Altera
 - Advantages of eBooks Over Traditional Books
2. Identifying 6 Uart Core Altera
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an 6 Uart Core Altera
 - User-Friendly Interface
4. Exploring eBook Recommendations from 6 Uart Core Altera
 - Personalized Recommendations
 - 6 Uart Core Altera User Reviews and Ratings

- 6 Uart Core Altera and Bestseller Lists
- 5. Accessing 6 Uart Core Altera Free and Paid eBooks
 - 6 Uart Core Altera Public Domain eBooks
 - 6 Uart Core Altera eBook Subscription Services
 - 6 Uart Core Altera Budget-Friendly Options
- 6. Navigating 6 Uart Core Altera eBook Formats
 - ePub, PDF, MOBI, and More
 - 6 Uart Core Altera Compatibility with Devices
 - 6 Uart Core Altera Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of 6 Uart Core Altera
 - Highlighting and Note-Taking 6 Uart Core Altera
 - Interactive Elements 6 Uart Core Altera
- 8. Staying Engaged with 6 Uart Core Altera
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers 6 Uart Core Altera
- 9. Balancing eBooks and Physical Books 6 Uart Core Altera
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection 6 Uart Core Altera
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine 6 Uart Core Altera
 - Setting Reading Goals 6 Uart Core Altera
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of 6 Uart Core Altera
 - Fact-Checking eBook Content of 6 Uart Core Altera
 - Distinguishing Credible Sources

13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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