

Active Matrix Driving and Circuit Simulation

Makoto Watanabe
Sony Mobile Display Corporation
Japan

1. Introduction

This chapter explains the principle of active matrix driving which is the most popular driving method used in current liquid crystal displays (LCDs). It then discusses issues that designers must overcome to avoid the malfunctioning and introduces a liquid crystal model for conducting circuit simulations to optimize the circuit parameters efficiently.

1.1 Equivalent circuit of a pixel in LCDs

The equivalent circuit of a pixel operated by active matrix driving is shown in Fig. 1. Data lines are connected to a data driver for generating the signal pulses for the picture data. Scan lines are connected to a scan driver for generating the scan pulses which enable the addressing driving. V_{sig} and V_g are applied to the data lines and scan lines, respectively. The thin film transistor (TFT) has three terminals of MOS transistors, and each terminal gate, drain, and source is connected to a scan line, a data line, and a pixel electrode, respectively. C_{gs} means the parasitic capacitance between the gate and source terminal in the TFT. Liquid crystal is injected into the gap between the pixel electrode and the counter backplane electrode, and it forms a liquid crystal cell capacitance (C_{lc}). C_{lc} is a variable capacitor that changes value according to the applied voltage between the pixel electrode and a counter backplane electrode. The voltage of the pixel electrode and counter backplane electrode are denoted by V_{pix} and V_{com} , respectively. The storage capacitor is denoted C_{sc} , and it is connected in parallel to C_{lc} . Its function is to hold charges on a pixel electrode while the TFT is switched off.

1.2 Timing chart for each signal pulse

Fig. 2 shows the wave forms applied to each bus line and electrode. The period during which the pixel electrode voltage (V_{pix}) is higher than the counter electrode voltage (V_{com}) is called the "plus frame" (Fig.2 (a)), whereas the period during which V_{pix} is lower than V_{com} is called the "minus frame" (Fig.2 (b)). The plus and minus frames are switched every frame period (T_f).

When the voltage of the gate terminal connecting to the scan line rise to a high level, the resistance between the drain and source terminals becomes very low (R_{on}). As a result, electrical charges flow into the pixel electrode from the data line till the voltage of the pixel electrode achieves the voltage of the data line during the writing time (T_w). This process is called the "Charge Process". When the voltage of the scan line starts to drop, the pixel electrode voltage shows a negative shift ΔV_{fd} because of the coupling with the gate terminal

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Table of Contents Active Matrix Driving And Circuit Simulation Intech

1. Understanding the eBook Active Matrix Driving And Circuit Simulation Intech
 - The Rise of Digital Reading Active Matrix Driving And Circuit Simulation Intech
 - Advantages of eBooks Over Traditional Books
2. Identifying Active Matrix Driving And Circuit Simulation Intech
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Active Matrix Driving And Circuit Simulation Intech
 - User-Friendly Interface
4. Exploring eBook Recommendations from Active Matrix Driving And Circuit Simulation Intech

- Personalized Recommendations
 - Active Matrix Driving And Circuit Simulation Intech User Reviews and Ratings
 - Active Matrix Driving And Circuit Simulation Intech and Bestseller Lists
5. Accessing Active Matrix Driving And Circuit Simulation Intech Free and Paid eBooks
 - Active Matrix Driving And Circuit Simulation Intech Public Domain eBooks
 - Active Matrix Driving And Circuit Simulation Intech eBook Subscription Services
 - Active Matrix Driving And Circuit Simulation Intech Budget-Friendly Options
 6. Navigating Active Matrix Driving And Circuit Simulation Intech eBook Formats
 - ePub, PDF, MOBI, and More
 - Active Matrix Driving And Circuit Simulation Intech Compatibility with Devices
 - Active Matrix Driving And Circuit Simulation Intech Enhanced eBook Features
 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Active Matrix Driving And Circuit Simulation Intech
 - Highlighting and Note-Taking Active Matrix Driving And Circuit Simulation Intech
 - Interactive Elements Active Matrix Driving And Circuit Simulation Intech
 8. Staying Engaged with Active Matrix Driving And Circuit Simulation Intech
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Active Matrix Driving And Circuit Simulation Intech
 9. Balancing eBooks and Physical Books Active Matrix Driving And Circuit Simulation Intech
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Active Matrix Driving And Circuit Simulation Intech
 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
 11. Cultivating a Reading Routine Active Matrix Driving And Circuit Simulation Intech
 - Setting Reading Goals Active Matrix Driving And Circuit Simulation Intech
 - Carving Out Dedicated Reading Time
 12. Sourcing Reliable Information of Active Matrix Driving And Circuit Simulation Intech

- Fact-Checking eBook Content of Active Matrix Driving And Circuit Simulation Intech
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
- Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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