Model Description （TensorFlow）

Symbolic Compiler

Model Mapper

Kernel Schedule

Kernel Configuration

SW Generator

HW Generator

C++ Codes

IIW Codes

C++ Compiler

Synthesis Tools

C++ Program

Programming File

Host

PCI-e Bus

Device

FPGA

DRAM

Fig. 1: FP-DNN Framework

# Fp Dnn An Automated Framework For Mapping Deep Neural

**Richard Bailey**

**Fp Dnn An Automated Framework For Mapping Deep Neural:**

*Robotic Computing on FPGAs* Shaoshan Liu,Zishen Wan,Bo Yu,Yu Wang,2022-05-31 This book provides a thorough overview of the state of the art field programmable gate array FPGA based robotic computing accelerator designs and summarizes their adopted optimized techniques This book consists of ten chapters delving into the details of how FPGAs have been utilized in robotic perception localization planning and multi robot collaboration tasks In addition to individual robotic tasks this book provides detailed descriptions of how FPGAs have been used in robotic products including commercial autonomous vehicles and space exploration robots      Network and Parallel Computing Shaoshan Liu,Xiaohui Wei,2022-11-30 This book constitutes the proceedings of the 19th IFIP WG 10 3 International Conference on Network and Parallel Computing NPC 2022 which was held in Jinan China during September 24 25 2022 The 23 full papers and 8 short papers presented in this volume were carefully reviewed and selected from 89 submissions They were organized in topical sections as follows computer architecture cloud computing deep learning emerging applications and storage and IO

**Embedded Computer Systems: Architectures, Modeling, and Simulation** Luigi Carro,Francesco Regazzoni,Christian Pilato,2025-01-27 The two volume set LNCS 15226 and 15227 constitutes the refereed proceedings of the 24th International Conference on Embedded Computer Systems Architectures Modeling and Simulation SAMOS 2024 held in Samos Greece during June 29 July 4 2024 The 24 full papers 10 invited full papers and 4 poster papers included in the proceedings were carefully reviewed and selected from 57 submissions They deal with embedded computer systems focusing on their applications architectures and underlying processors as well as methods created to automate their design

**Applied Reconfigurable Computing. Architectures, Tools, and Applications** Fernando Rincón,Jesús Barba,Hayden K. H. So,Pedro Diniz,Julián Caba,2020-03-25 This book constitutes the proceedings of the 16th International Symposium on Applied Reconfigurable Computing ARC 2020 held in Toledo Spain in April 2020 The 18 full papers and 11 poster presentations presented in this volume were carefully reviewed and selected from 40 submissions The papers are organized in the following topical sections design methods design space exploration high level synthesis architectures applications

Applied Reconfigurable Computing. Architectures, Tools, and Applications Steven Derrien,Frank Hannig,Pedro C. Diniz,Daniel Chillet,2021-06-23 This book constitutes the proceedings of the 17th International Symposium on Applied Reconfigurable Computing ARC 2021 held as a virtual event in June 2021 The 14 full papers and 11 short presentations presented in this volume were carefully reviewed and selected from 40 submissions The papers cover a broad spectrum of applications of reconfigurable computing from driving assistance data and graph processing acceleration computer security to the societal relevant topic of supporting early diagnosis of Covid infectious conditions      *Innovations in Smart Cities Applications Volume 5* Mohamed Ben Ahmed,Anouar Abdelhakim Boudhir,İsmail Rakıp Karaş,Vipul Jain,Sehl Mellouli,2022-03-03 This book sets the innovative research contributions works and solutions for almost all the intelligent

and smart applications in the smart cities The smart city concept is a relevant topic for industrials governments and citizens Due to this the smart city considered as a multi domain context attracts tremendously academics researchers and practitioners who provide efforts in theoretical proofs approaches architectures and in applied researches The importance of smart cities comes essentially from the significant growth of populations in the near future which conducts to a real need of smart applications that can support this evolution in the future cities The main scope of this book covers new and original ideas for the next generations of cities using the new technologies The book involves the application of the data science and AI IoT technologies and architectures smart earth and water management smart education and E learning systems smart modeling systems smart mobility and renewable energy It also reports recent research works on big data technologies image processing and recognition systems and smart security and privacy *Proceedings of Ninth International Congress on Information and Communication Technology* Xin-She Yang,Simon Sherratt,Nilanjan Dey,Amit Joshi,2024-07-29 This book gathers selected high quality research papers presented at the Ninth International Congress on Information and Communication Technology held in London on February 19 22 2024 It discusses emerging topics pertaining to information and communication technology ICT for managerial applications e governance e agriculture e education and computing technologies the Internet of Things IoT and e mining Written by respected experts and researchers working on ICT the book offers an asset for young researchers involved in advanced studies The work is presented in ten volumes *Techniques for Mapping Deep Neural Network Frameworks to Programmable Accelerators* Stefan Hadjis,2021 The trend towards increasing specialization in DNN accelerators is first discussed as well as why FPGA hardware is sometimes selected The two major ways that DNN applications can be automatically mapped to FPGAs are then reviewed 1 mapping to manually optimized template designs or overlay architectures which is suited to DNN frameworks as a mapping source and 2 mapping by compiling automatically designed hardware Next an open source end to end toolchain to map TensorFlow DNNs to cloud FPGAs is described which is the first open source toolchain to use a modern DNN framework as a starting point and either 1 target public cloud FPGA hardware or 2 compile DNNs reaching state of the art accuracy on an FPGA cloud or not This compiler is used to explore tradeoffs in DNN to FPGA mapping including tensor storage format and architecture specialization and to examine how different layer dimensions and other characteristics such as locality affect design decisions Next optimizations to improve circuits automatically designed by hardware compilation tools and DSLs are investigated An algorithm for high level hardware compilers is presented which reduces resource utilization for on chip memory accesses common in DNNs and computer vision Its applicability to general dense access patterns and applications is also demonstrated For each of these observations generalization is made beyond DNN or ML domains and examples are shown where increasing specialization or heterogeneity in storage formats processor architecture and on chip data structures can improve FPGA accelerator resource utilization timing closure and bandwidth requirements **Framework**

**for Mapping Convolutional Neural Networks on FPGAs** Masoud Shahshahani,2021 Artificial Intelligence AI applications are on the rise Recent advances in machine learning and deep learning have created various applications for medicine healthcare financial markets security entertainment and social sciences Deep Learning especially has demonstrated tremendous opportunities in computer vision autonomous driving natural language processing and many more Deep learning allows machines to solve complex problems using Artificial Neural Networks ANNs and the learning itself can be supervised or semisupervised Multilayered artificial neural networks are called Deep Neural Networks DNNs These deep computational models are composed of multiple sequentially processing layers that help learn the representations within a given data set Convolutional Neural Networks CNN are a particular class of deep networks that use convolution to extract features from usually a time domain or frequency domain data and then use the extracted features to classify that data for final inferencing Several software tools and frameworks are available to facilitate the deep learning community with the fast development and high performance execution of DNNs Tool flows such as PyTorch Caffe Theano and TensorFlow aim to increase the productivity of CNN software developers by providing a pathway for implementing deep networks on high performance multi core CPUs GPUs and DSPs GPUs especially provide easy access to floating point operations and also allow very high memory bandwidths Some of the latest Nvidia GPUs Nvidia GeForce RTX2080 consume as much as 300 watts of power Excessive power dissipation can make GPUs an unfavorable candidate for implementing CNNs for a variety of applications Field Programmable Gate Arrays FPGAs provide a high degree of customized parallelization and offer far superior performance per watt We believe that FPGA based accelerators are ideal platforms for implementing Convolutional Neural Networks for computer vision and related applications Software engineers with minimal hardware design skills demand tremendous support within the tool flows and FPGA vendors are fully embracing new methodologies like high level synthesis where the designs can be described as a program written in languages like C C However commercial FPGAs are resource scarce the CNN mapping design space is enormous and efficient mapping of CNN can quickly become a challenging task The requirement of FPGA resources latency and power is affected by many parameters including the CNN architecture and the level of computational parallelism In practice a software designer first explores various CNN architectures in software to improve architecture0 9s validation accuracy Once an architecture has been finalized the designer ports the architecture design to FPGA for inference acceleration The mapping process undergoes performance optimization by tweaking many design related parameters during the design space exploration and changing the operating frequencies The entire process is highly time consuming This dissertation describes a fully automated end to end design framework for implementing CNNs on FPGAs The framework allows a designer to express the CNNs in commonly preferred Python language descriptions and provides a guided tool flow to generate a custom Intellectual Property IP block In addition the framework allows easy and complete exploration for selecting final design implementations based on optimization parameters that include Performance

Power and Area PPA **Efficient Processing of Deep Neural Networks** Vivienne Sze,Yu-Hsin Chen,Tien-Ju Yang,Joel S. Emer,2022-05-31 This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks DNNs DNNs are currently widely used for many artificial intelligence AI applications including computer vision speech recognition and robotics While DNNs deliver state of the art accuracy on many AI tasks it comes at the cost of high computational complexity Therefore techniques that enable efficient processing of deep neural networks to improve key metrics such as energy efficiency throughput and latency without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems The book includes background on DNN processing a description and taxonomy of hardware architectural approaches for designing DNN accelerators key metrics for evaluating and comparing different designs features of DNN processing that are amenable to hardware algorithm co design to improve energy efficiency and throughput and opportunities for applying new technologies Readers will find a structured introduction to the field as well as formalization and organization of key concepts from contemporary work that provide insights that may spark new ideas **Deep Neural Evolution** Hitoshi Iba,Nasimul Noman,2020-05-21 This book delivers the state of the art in deep learning DL methods hybridized with evolutionary computation EC Over the last decade DL has dramatically reformed many domains computer vision speech recognition healthcare and automatic game playing to mention only a few All DL models using different architectures and algorithms utilize multiple processing layers for extracting a hierarchy of abstractions of data Their remarkable successes notwithstanding these powerful models are facing many challenges and this book presents the collaborative efforts by researchers in EC to solve some of the problems in DL EC comprises optimization techniques that are useful when problems are complex or poorly understood or insufficient information about the problem domain is available This family of algorithms has proven effective in solving problems with challenging characteristics such as non convexity non linearity noise and irregularity which dampen the performance of most classic optimization schemes Furthermore EC has been extensively and successfully applied in artificial neural network ANN research from parameter estimation to structure optimization Consequently EC researchers are enthusiastic about applying their arsenal for the design and optimization of deep neural networks DNN This book brings together the recent progress in DL research where the focus is particularly on three sub domains that integrate EC with DL 1 EC for hyper parameter optimization in DNN 2 EC for DNN architecture design and 3 Deep neuroevolution The book also presents interesting applications of DL with EC in real world problems e g malware classification and object detection Additionally it covers recent applications of EC in DL e g generative adversarial networks GAN training and adversarial attacks The book aims to prompt and facilitate the research in DL with EC both in theory and in practice **A Framework for FPGA-based Acceleration of Neural Network Inference with Limited Numerical Precision Via High-level Synthesis with Streaming Functionality** Ruo Long Lian,2016 *Efficient Implementation of Deep Neural Networks on*

*Resource-constrained Devices* Maedeh Hemmat,2022 In recent years Deep Neural Networks DNNs have emerged as an impressively successful model to perform complicated tasks including object classification speech recognition autonomous vehicle etc To provide better accuracy state of the art neural network models are designed to be deeper i e having more layers and larger i e having more parameters within each layer It subsequently has increased the computational and memory costs of DNNs mandating their efficient hardware implementation especially on resource constrained devices such as embedded systems and mobile devices This challenge can be investigated from two aspects computation and storage On one hand state of the art DNNs require the execution of billions of operations for each inference This is while the computational power of embedded systems is tightly limited On the other hand DNN models require storage of several Megabytes of parameters which can t fit in the on chip memory of these devices More importantly these systems are usually battery powered with a limited energy budget to access memory and perform computations This dissertation aims to make contributions towards improving the efficiency of DNN deployments on resource constraint devices Our contributions can be categorized into three aspects First we propose an iterative framework that enables dynamic reconfiguration of an already trained Convolutional Neural Network CNN in hardware during inference The reconfiguration enables input dependent approximation of the CNN at run time leading to significant energy savings without any significant degradation in classification accuracy Our proposed framework breaks each inference into several iterations and fetches only a fraction of the weights from off chip memory at each iteration to perform the computations It then decides to either terminate the network or fetch more weights to do the inference based on the difficulty of the received input The termination condition can be also adjusted to trade off classification accuracy and energy consumption at run time Second we exploit the user dependent behavior of DNNs and propose a personalized inference framework that prunes an already trained neural network model based on the preferences of individual users and without the need to retrain the network Our key observation is that an individual user may only encounter a tiny fraction of the trained classes on a regular basis Hence storing trained models pruned or not for all possible classes on local devices is costly and unnecessary for the user s needs Our personalized framework minimizes the memory computation and energy consumption of the network on the local device as it processes neurons on a need basis i e only when the user expects to encounter a specific output class Third we propose a framework for distributed inference of DNNs across multiple edge devices to improve the communication and latency overheads Our framework utilizes many parallel independent running edge devices which communicate only once to a single back end device also an edge device to aggregate their predictions and produce the result of the inference To achieve this distributed implementation our framework first partitions the classes of the complex DNN into subsets to be assigned across the available edge devices while considering the computational resources of each device The DNN is then aggressively pruned for each device for its set of assigned classes Each smaller DNN SNN is further configured to return a Don t Know when

encountered by an input from an unassigned class Each SNN is generated from the complex DNN at the beginning and then loaded onto its corresponding edge device without the need for retraining To perform inference each SNN will perform an inference based on its received input      Design Space Exploration and Architecture Design for Inference and Training Deep Neural Networks Yangjie Qi,2021 Deep Neural Networks DNNs are widely used in various application domains and achieve remarkable results However DNNs require a large number of computations for both the inference and training phases Hardware accelerators are designed and implemented to compute DNN models efficiently Many accelerators have been proposed for DNN inference while only a limited set of DNN training accelerators has been proposed Almost all of these accelerators are highly custom designed and limited in the types of networks they can process This dissertation focuses on designing novel architectures and tools for efficient training of deep neural networks particularly for edge applications We proposed several novel architectures and a design space exploration tool Our proposed architecture can be used for efficient processing of DNNs and the design space exploration model could help DNN architects explore the design space of DNN architecture design for both inference and training and help home in on the optimal architecture in different hardware constraints in applications The first area of contribution in this dissertation is the design of Socrates D 1 a digital multicore on chip learning architecture for deep neural networks This processing unit design demonstrates the capability to process the training phase of DNNs efficiently A statically time multiplexed routing mechanism and a co designed mapping method are also introduced to improve overall throughput and energy efficiency The experimental results show 6 8 to 22 3 times speedup and more than a thousand times energy efficiency over a GPGPU The proposed architecture is also compared with several DNN training accelerators and achieves the best energy and area efficiencies The second area of contribution in this dissertation is the design of Socrates D 2 which is an enhanced version of Socrates D 1 This architecture presents a novel neural processing unit design A dual ported eDRAM memory replaces the double eDRAM memory design used in Socrates D 1 In addition a new mapping method utilizing neural network pruning techniques is introduced and evaluated with several datasets The co designed mapping methods helped the architecture achieve both throughput and energy efficiency without loss of accuracy Compared with Socrates D 1 this new architecture shows an average of 1 2 times higher energy efficiency and 1 25 times better area efficiency The third area of contribution in this dissertation is the development of TRIM a design space exploration model for DNN accelerators TRIM is an infrastructure model and can explore the design space of DNN accelerators for training and inference It utilizes a very flexible hardware template which can model a wide range of architectures TRIM explores the design space of data partition and reuse strategies for each hardware architecture and estimates the optimal time and energy Our experimental results show that TRIM can achieve more than eighty percent accuracy on time and energy estimations To the best of our knowledge TRIM is the first infrastructure to model and explore the design space of DNN accelerators for training and inference The fourth area of contribution in this dissertation is a set of

design space explorations using TRIM Through several case studies we explored the design space of DNN accelerators for training and inference We compared different dataflows and showed the impact of dataflow on efficient processing DNNs We showed how to use TRIM to optimize the dataflow We explored the design space of spatial architectures and showed the results of varying different hardware choices Based on the exploration results several high throughput and energy efficient DNN training accelerators were presented The fifth area of contribution in this dissertation is the design of an FPGA based training accelerator for edge devices We designed a CPU FPGA accelerator that can operate under 5W TRIM is utilized for dataflow optimization and hardware parameter selection The experimental results show that we could achieve a 1 93 times speedup and 1 43 times energy efficiency for end to end training over a CPU implementation

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