

Tanner EDA Releases T-Spice

Pasadena, Calif.--Feb. 23, 1998-- Tanner EDA (Pasadena) announced the V5 release of the T-Spice Pro integrated circuit design capture and simulation system for Windows 95 and NT. The tool suite includes the S-Edit schematic editor, the T-Spice circuit simulator, and the W-Edit waveform viewer. The new release includes improvements in user interface, integration, and simulation and modeling technology.

Tanner's hierarchic schematic capture tool, S-Edit, has been overhauled to add many new Windows 95 and NT user interface improvements. Other enhancements include a superior simulation interface and more flexible design export capabilities. A new browser gives quick access to cell library components. Library files can be easily added, removed, or accessed for design reuse. A "quick pick" feature gives fast access to frequently used components.

S-Edit is well integrated with the T-Spice circuit simulator and W-Edit waveform viewer. Simulation results can be viewed by probing the schematic using the new waveform probing feature. New design export features include support for parametric subcircuits, control of subcircuit pin orders, and output in EDIF 2.0.0 and VHDL formats. Compatibility with L-Edit simplifies the design process--there is no longer a need to use mismatched design capture, simulation, and layout tools.

Tanner's circuit simulator, T-Spice, contains the BSIM3v3.1 MOSFET model, the latest version of Berkeley's BSIM3 model. New MESFET models have also been added for GaAs IC support. T-Spice accepts the latest parasitic and size-based device characterization data available from foundries to give accurate simulation results.

For devices that cannot be represented by one of T-Spice's internal models, custom models can be written using a new external model interface. Written in the C programming language, external models can be simulated using a built-in C-interpreter, or compiled into a dynamically linked library (DLL). The general purpose interface allows the addition of functional and behavioral level models in addition to custom transistor models.

T-Spice's new enhanced Fourier analysis command contains new accuracy and output control options. A waveform relaxation engine has been added as an alternative to the standard transient analysis method for simulation of large circuits. Simulation queuing is also supported for running multiple T-Spice analyses. Several new commands and options have been added to control simulation methods, output data compression, case sensitivity, device scaling, output expression handling, and simulation statistics. In addition, T-Spice's netlist manipulation tools have been enhanced with undo and redo, and regular expression search and replace capabilities.

Additions to W-Edit improve the power and flexibility for graphically viewing simulation output data. New controls provide precise adjustment of the graphical display of output data. A waveform arithmetic tool can display traces formed by writing mathematical expressions. Traces defined by expressions can be composed of arithmetic combinations of other trace names or can

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AW Rasmussen



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