

Chapter 5: Processor fundamentals: Answers to coursebook questions and to Worksheet questions

Syllabus section covered: 4.1

From the coursebook

Extension question 5.01

- 1 Memory capacity, hard disk capacity and processor clock speed.

Note that almost certainly the GB and TB will be based on the old-fashioned use of $1K = 1024$.

- 2 A clock speed of 1.7 GHz implies $1 \div (1.7 \times 10^9)$ s as the time between clock signals. This is 5.9×10^{-10} s, which is the minimum time period that could separate successive activities.

Extension question 5.02

There is no correct answer here. It is possible that your technical staff can provide some technical specification data.

Exam-style Questions

- 1 a Accumulator (1)
- b i It stores the address of a memory location or an I/O component about to be used (for reading or writing). (1)
- ii An address as a binary value. (1)
- iii The program counter (PC). (1)
- c i It holds the instruction currently being executed. (1)
- ii An instruction in a binary representation. (1)
- iii Memory data register/memory buffer register (no marks given for acronyms). (1)
- d 1 mark each for any of the following. (max 5)
- MDR contains a binary code that has been retrieved from memory using the data bus, may be a datum, an address or an instruction, acts as a buffer to handle different speeds within the CPU and on the data bus.
 - MAR contains an address used to identify the memory location where data is to be stored or from where data is to be retrieved, the address is transferred to the MAR from the PC
- 1 mark for each of the following. (max 6)

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JA Banks



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