

FPGA INTERVIEW QUESTIONS

What is FPGA ?

A field-programmable gate array is a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects. Logic blocks can be programmed to perform the function of basic logic gates such as AND, and XOR, or more complex combinational functions such as decoders or mathematical functions. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. A hierarchy of programmable interconnects allows logic blocks to be interconnected as needed by the system designer, somewhat like a one-chip programmable breadboard. Logic blocks and interconnects can be programmed by the customer or designer, after the FPGA is manufactured, to implement any logical function—hence the name "field-programmable". FPGAs are usually slower than their application-specific integrated circuit (ASIC) counterparts, cannot handle as complex a design, and draw more power (for any given semiconductor process). But their advantages include a shorter time to market, ability to re-program in the field to fix bugs, and lower non-recurring engineering costs. Vendors can sell cheaper, less flexible versions of their FPGAs which cannot be modified after the design is committed. The designs are developed on regular FPGAs and then migrated into a fixed version that more resembles an ASIC.

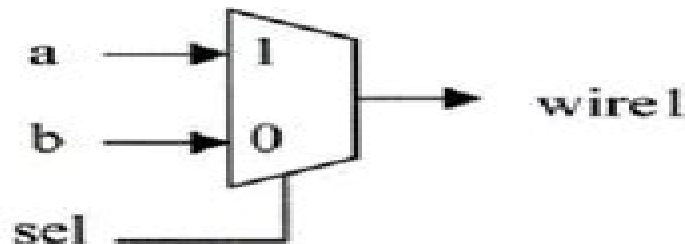
What logic is inferred when there are multiple assign statements targeting the same wire?

It is illegal to specify multiple assign statements to the same wire in a synthesizable code that will become an output port of the module. The synthesis tools give a syntax error that a net is being driven by more than one source. However, it is legal to drive a three-state wire by multiple assign statements.

What do conditional assignments get inferred into?

Conditionals in a continuous assignment are specified through the "?" operator. Conditionals get inferred into a multiplexor. For example, the following is the code for a simple multiplexor

```
assign wire1 = (sel==1'b1) ? a : b;
```



What value is inferred when multiple procedural assignments made to the same reg variable in an always block?

Fpga Interview Questions Asic

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Table of Contents Fpga Interview Questions Asic

1. Understanding the eBook Fpga Interview Questions Asic
 - The Rise of Digital Reading Fpga Interview Questions Asic
 - Advantages of eBooks Over Traditional Books
2. Identifying Fpga Interview Questions Asic
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Fpga Interview Questions Asic
 - User-Friendly Interface
4. Exploring eBook Recommendations from Fpga Interview Questions Asic
 - Personalized Recommendations
 - Fpga Interview Questions Asic User Reviews and Ratings
 - Fpga Interview Questions Asic and Bestseller Lists
5. Accessing Fpga Interview Questions Asic Free and Paid eBooks
 - Fpga Interview Questions Asic Public Domain eBooks
 - Fpga Interview Questions Asic eBook Subscription Services
 - Fpga Interview Questions Asic Budget-Friendly Options

6. Navigating Fpga Interview Questions Asic eBook Formats
 - ePub, PDF, MOBI, and More
 - Fpga Interview Questions Asic Compatibility with Devices
 - Fpga Interview Questions Asic Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Fpga Interview Questions Asic
 - Highlighting and Note-Taking Fpga Interview Questions Asic
 - Interactive Elements Fpga Interview Questions Asic
8. Staying Engaged with Fpga Interview Questions Asic
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Fpga Interview Questions Asic
9. Balancing eBooks and Physical Books Fpga Interview Questions Asic
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Fpga Interview Questions Asic
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine Fpga Interview Questions Asic
 - Setting Reading Goals Fpga Interview Questions Asic
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Fpga Interview Questions Asic
 - Fact-Checking eBook Content of Fpga Interview Questions Asic
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements

- Interactive and Gamified eBooks

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