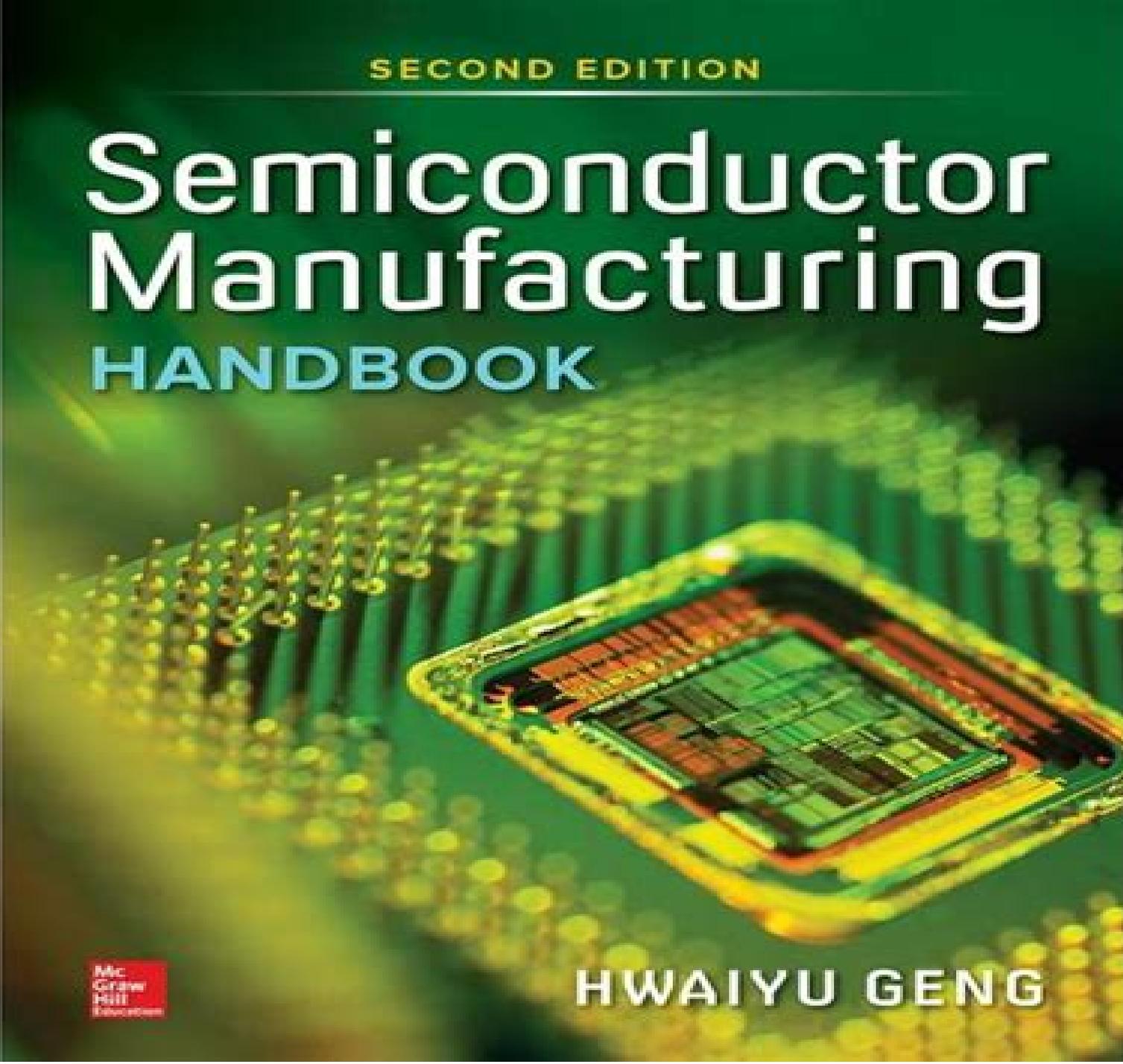


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Silicon Nitride, Silicon Dioxide, and Emerging Dielectrics 9 R. Ekwah Sah, 2007 This issue of ECS Transactions contains the papers presented in the symposium on Silicon Nitride, Silicon Dioxide, Thin Insulating Films, and Emerging Dielectrics held May 6-11, 2007 in Chicago. Papers were presented on deposition, characterization, and applications of the dielectrics, including

high and low k dielectrics as well as interface states device characterization reliability and modeling Reliability of high-k / metal gate field-effect transistors considering circuit operational constraints Steve Kupke,2016-06-06 After many decades the scaling of silicon dioxide based field effect transistors has reached insurmountable physical limits due unintentional high gate leakage currents for gate oxide thicknesses below 2 nm The introduction of high k metal gate stacks guaranteed the trend towards smaller transistor dimensions The implementation of HfO₂ as high k dielectric also lead to a substantial number of manufacturing and reliability challenges The deterioration of the gate oxide properties under thermal and electric stress jeopardizes the circuit operation and hence needs to be comprehensively understood As a starting point 6T static random access memory cells were used to identify the different single device operating conditions The strongest deterioration of the gate stack was found for nMOS devices under positive bias temperature instability PBTI stress resulting in a severe threshold voltage shift and increased gate leakage current A detailed investigation of physical origin and temperature and voltage dependency was done The reliability issues were caused by the electron trapping into already existing HfO₂ oxygen vacancies The oxygen vacancies reside in different charge states depending on applied stress voltages This in return also resulted in a strong threshold voltage and gate current relaxation after stress was cut off The reliability assessment using constant voltage stress does not reflect realistic circuit operation which can result in a changed degradation behaviour Therefore the constant voltage stress measurement were extended by considering CMOS operational constraints where it was found that the supply voltage frequently switches between the gate and drain terminal The additional drain off state bias lead to an increased V_t relaxation in comparison to zero bias voltage The off state influence strongly depended on the gate length and became significant for short channel devices The influence of the off state bias on the dielectric breakdown was studied and compared to the standard assessment methods Different wear out mechanisms for drain only and alternating gate and drain stress were verified Under drain only stress the dielectric breakdown was caused by hot carrier degradation The lifetime was correlated with the device length and amount of subthreshold leakage The gate oxide breakdown under alternating gate and o state stress was caused by the continuous trapping and detrapping behaviour of high k metal gate devices Handbook Of Semiconductor Manufacturing Technology Y. Nishi,2000 **Handbook of Production**

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