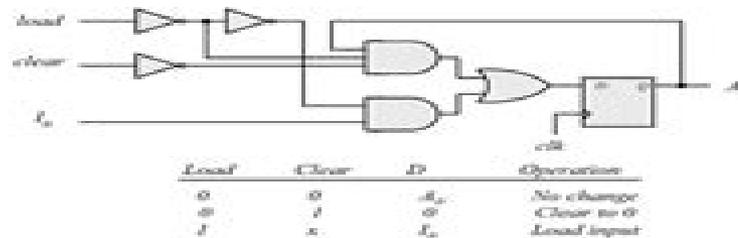


CHAPTER 6

- 6.1** The structure shown below gates the clock through a nand gate. In practice, the circuit can exhibit two problems if the load signal is asynchronous: (1) the gated clock arrives in the setup interval of the clock of the flip-flop, causing metastability, and (2) the load signal truncates the width of the clock pulse. Additionally, the propagation delay through the nand gate might compromise the synchronicity of the overall circuit.



- 6.2** Modify Fig. 6.2, with each stage replicating the first stage shown below:



Note: In this design, *load* has priority over *clear*.

- 6.3** Serial data is transferred one bit at a time. Parallel data is transferred n bits at a time ($n > 1$).
- A shift register can convert serial data into parallel data by first shifting one bit a time into the register and then taking the parallel data from the register outputs.
- A shift register with parallel load can convert parallel data to a serial format by first loading the data in parallel and then shifting the bits one at a time.
- 6.4** 101101 \Rightarrow 1101; 0110; 1011; 1101; 0110; 1011
- 6.5** (a) See Fig. 11.19: IC 74194
- (b) See Fig. 11.20. Connect two 74194 ICs to form an 8-bit register.

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