

# Computer Architecture 1 Final Exam

ELE319, Hanyang University, 2019 Spring.  
ID: \_\_\_\_\_ Name: \_\_\_\_\_

Department: \_\_\_\_\_

The first two problems are mandatory. If you fail to answer the questions, you will not receive any credit.

1. (5pt) Specify the 5-stage pipeline and explain what operation is performed at each stage.
2. (5pt) Specify three hazards in processor pipelining and explain hardware and software approaches to solve the hazards.
3. (5pt) Write the output value (C) for the given circuits if  $A=1$  and  $B=1$ .



4. (5pt) We construct a 2-bit multiplier using Mux as following. Two inputs are provided to a selector in Mux. For instance,  $01 * 01 = 0001$  and  $00 * 00 = 0000$  in the following figure. Fill the remained constant input values in the Mux to complete the multiplier. (1.5pt)



5. (5pt) Similarly, we are constructing a divider using a ROM as following. In the example, if dividend is 5 and divisor is 2 then quotient is 2 and remainder is 1. Hence,  $0x21$  is stored at address  $0x52$ . What value should be stored at address  $0x53$  in the ROM to support the divider? (1.5pt)



6. (5pt) What is the difference between latch and flip-flop? (5pt)
7. (5pt) For the following arithmetic unit, we want to compute  $A-B$  where 2's complement number is used. Determine proper values for  $S1, S0, Cin$  to make  $F = A-B$ .



8. (24pt) The following figure shows single cycle implementation for datapath and control path for MIPS architecture.



Fill 0, 1 or X(don't care) in the following table to implement for the architecture.

Instruction	ALU Op	MEMOp	Reg Write	Mem Read	Mem Write	Branch
R-type instruction	(1)	(2)	(3)	(4)	(5)	(6)
Load	(7)	(8)	(9)	(10)	(11)	(12)
Store	(13)	(14)	(15)	(16)	(17)	(18)
branch	(19)	(20)	(21)	(22)	(23)	(24)

# Computer Architecture Exam Solutions

**Y Pai**



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### **Table of Contents Computer Architecture Exam Solutions**

1. Understanding the eBook Computer Architecture Exam Solutions
  - The Rise of Digital Reading Computer Architecture Exam Solutions
  - Advantages of eBooks Over Traditional Books
2. Identifying Computer Architecture Exam Solutions
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in a Computer Architecture Exam Solutions
  - User-Friendly Interface
4. Exploring eBook Recommendations from Computer Architecture Exam Solutions
  - Personalized Recommendations
  - Computer Architecture Exam Solutions User Reviews and Ratings

- Computer Architecture Exam Solutions and Bestseller Lists
- 5. Accessing Computer Architecture Exam Solutions Free and Paid eBooks
  - Computer Architecture Exam Solutions Public Domain eBooks
  - Computer Architecture Exam Solutions eBook Subscription Services
  - Computer Architecture Exam Solutions Budget-Friendly Options
- 6. Navigating Computer Architecture Exam Solutions eBook Formats
  - ePub, PDF, MOBI, and More
  - Computer Architecture Exam Solutions Compatibility with Devices
  - Computer Architecture Exam Solutions Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Computer Architecture Exam Solutions
  - Highlighting and Note-Taking Computer Architecture Exam Solutions
  - Interactive Elements Computer Architecture Exam Solutions
- 8. Staying Engaged with Computer Architecture Exam Solutions
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Computer Architecture Exam Solutions
- 9. Balancing eBooks and Physical Books Computer Architecture Exam Solutions
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Computer Architecture Exam Solutions
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine Computer Architecture Exam Solutions
  - Setting Reading Goals Computer Architecture Exam Solutions
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Computer Architecture Exam Solutions
  - Fact-Checking eBook Content of Computer Architecture Exam Solutions
  - Distinguishing Credible Sources

13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
  - Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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