Chapter 6 VLSI Testing

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Chapter 6 Vlsi Testing Ncu

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    <u>Advanced VLSI Design and Testability Issues</u> Suman Lata Tripathi,Sobhit Saxena,Sushanta Kumar Mohapatra,2020-08-18 This book facilitates the VLSI interested individuals with not only in depth knowledge but also the broad aspects of it by explaining its applications in different fields including image processing and biomedical The deep understanding of basic concepts gives you the power to develop a new application aspect which is very well taken care of in this book by using simple language in explaining the concepts In the VLSI world the importance of hardware description languages cannot be ignored as the designing of such dense and complex circuits is not possible without them Both Verilog and VHDL languages are used here for designing The current needs of high performance integrated circuits ICs including low power devices and new emerging materials which can play a very important role in achieving new functionalities are the most interesting part of the book The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era The role of fault simulation algorithms is very well explained and its implementation using Verilog is the key aspect of this book This book is well organized into 20 chapters Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications Then the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2 5 The performance enhancement with alternate material or geometry for silicon based FET designs is focused in Chapters 6 and 7 Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs Chapters 10 13 deal with advanced FET structures available in various shapes materials such as nanowire HFET and their comparison in terms of device performance metrics calculation Chapters 14 18 describe different application specific VLSI design techniques and challenges for analog and digital circuit designs Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC s structure and function which makes it much more difficult to reverse engineer   *On-Line Testing for VLSI* Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers   **Introduction to**

VLSI Testing Robert J. Feugate (jr.),Steven M. McIntyre,1988   *Tutorial--VLSI Testing & Validation Techniques* Hassan K. Reghbati,1985   VLSI Test Principles and Architectures Laung-Terng Wang,Cheng-Wen Wu,Xiaoqing Wen,2006-08-14 This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product drive down test cost improve product quality and yield and speed up time to market and time to volume Most up to date coverage of design for testability Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books Numerous practical examples in each chapter illustrating basic VLSI test principles and DFT architectures

    VLSI Test Principles and Architectures Laung-Terng Wang,Cheng-Wen Wu (EE Ph. D.),Xiaoqing Wen,2006 This book is a fundamental VLSI Testing and Design for Testability DFT textbook allowing undergraduates DFT practitioners and VLSI designers to learn quickly the basic VLSI Test concepts principles and architectures for test and diagnosis of digital memory and analog mixed signal designs VLSI Testing is very basic to the semiconductor industry and is something that almost everyone in the industry needs to have some knowledge of It is often not sufficiently covered in undergraduate curricula therefore this book fill the gap in this area for both students and professionals in semiconductor manufacturing design systems electronic design automation EDA etc As 100 million transistor designs are now common test costs are 25 40% of the overall cost of manufacturing a chip and how a chip is designed greatly impacts the cost of test As such it is important for designers and managers to understand the concepts and principles of testing and design for test techniques Covers the entire spectrum of VLSI testing from digital analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future test technology trends and challenges facing the nanometer design era Companion CD ROM contains a version of SynTest s software for student use   *Introduction to VLSI Testing* Robert J. Feugate,Steven M. McIntyre,1988   **VLSI Design** M. Michael Vai,2017-12-19 Very Large Scale Integration VLSI has become a necessity rather than a specialization for electrical and computer engineers This unique text provides Engineering and Computer Science students with a comprehensive study of the subject covering VLSI from basic design techniques to working principles of physical design automation tools to leading edge application specific array processors Beginning with CMOS design the author describes VLSI design from the viewpoint of a digital circuit engineer He develops physical pictures for CMOS circuits and demonstrates the top down design methodology using two design projects a microprocessor and a field programmable gate array The author then discusses VLSI testing and dedicates an entire chapter to the working principles strengths and weaknesses of ubiquitous physical design tools Finally he unveils the frontiers of VLSI He emphasizes its use as a tool to develop innovative algorithms and architecture to solve previously intractable problems VLSI Design answers not only the question of what is VLSI but also shows how to use VLSI It provides graduate and upper level undergraduate students with a complete and congregated view of VLSI engineering   **VLSI testing** T. W. Williams,1986   *VLSI Testing* T. W. Williams,1988   *VLSI Fault Modeling and Testing Techniques* George W. Zobrist,1993 VLSI systems are becoming

very complex and difficult to test Traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated ciruit Hierarchial models are needed that are easy to use at the transistor and functional levels Stuck open faults present severe testing problems in CMOS circuits to overcome testing problems testable designs are utilized Bridging faults are important due to the shrinking geometry of ICs BIST PLA schemes have common features controllability and observability which are enhanced through additional logic and test points Certain circuit topologies are more easily testable than others The amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty Test implementation is usually left until after the VLSI data path has been synthesized into a structural description This leads to investigation methodologies for performing design synthesis with test incorporation These topics and more are discussed *Tutorial--VLSI Testing & Validation Techniques* ,1985 **A Boundary Test Approach to VLSI Testing** Matthew Christopher Graf,1982 Built-in Testing Procedures for LSI/VLSI Circuits Vinod Kumar Sutravez,1984 Functional Testing of LSI/VLSI (Very Large Scale Integration) Based Systems with Measure of Fault Coverage Stephen Y. Su,STATE UNIV OF NEW YORK AT BINGHAMTON DEPT OF COMPUTER SCIENCE.,1983 Due to the advances in the integrated circuit IC technology more and more components are being fabricated into a tiny IC chip Since the number of pins on each chip is limited by the physical size of the chip the problem of testing becomes more difficult than ever especially in the VLSI Very Large Scale Integration chips This problem is aggravated by the fact that in nearly all cases integrated circuit manufacturers are not willing to release the detailed circuit diagram of the IC chip to the users Yet as users of the IC chips to make sure that the implemented system is reliable we need to test the IC chips and the systems made of the interconnection of these chips The purpose of this project is to find efficient algorithms for testing LSI VLSI chips and LSI VLSI based systems This report is organized into two chapters Chapter 1 presents the state of the art for the functional testing of LSI VLSI devices with special emphasis on microprocessor testing Chapter 2 reports our new research results We present three algorithms to test the instruction decoding function of microprocessors

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