

FPGA Implementation of Beamforming Receivers Based on MRC and NC-LMS for DS-CDMA System

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Abstract—In this paper, we investigate a beamforming receiver based on maximum ratio combining (MRC) and noise constrained least mean square (NC-LMS) using rapid prototyping method for FPGA implementation. Non-adaptive and adaptive beamforming techniques approaches are considered. A performance evaluation of these algorithms in a DS-CDMA system is presented and FPGA design is evaluated in terms of hardware resources for Xilinx family devices using rapid prototyping methodology with Matlab-Simulink tools. Both approaches offer a good performance-complexity tradeoff favorable for FPGA implementation. However, due to the adaptive approach, the NC-LMS presents a better robustness to the fixed point arithmetic than the MRC.

1. INTRODUCTION

THE need, the quest for high-performance, high-speed, high-quality, high-reliability and most importantly low-cost systems drives the engineers to different and unlimited frontiers of design and implementations. In this paper we face the problem of Beamforming or Smart Antennas (SA) design and implementation for DS-CDMA systems equipped with multiple receiving antennas.

SAs are recognized as a key technology for capacity increase in 3G radio networks. A SA's ability to abate both multipath and co-channel interference makes it one of the leading candidates [1] and one of the most promising technologies for the enabling of high capacity of the wireless networks, and interference cancellation. The most important contributions of an SA is its capability of changing its pattern in real time in order to track the user of interest with its maximum gain while trying to minimize the interference by placing the nulls of its radiation pattern at locations of the other users [2], i.e. the interferers.

Beamforming is the complex mathematical process standing behind that behavior of the antenna or the base station. We describe it as the backbone of the SA, or the main core of it. The beamforming is a process in which each user's signal is multiplied with appropriate weights that adjust the magnitude and the phase of the signal from each antenna. Hence the array forms a transmit beam in the desired direction and minimizes the output in other directions.

Considering the hardware implementation for beamforming algorithms, few past works have been reported. In [3], a reduced sampling rate beamforming technique for the reception of acoustic data transmitted through the water has been implemented on a DSP from Texas Instrument. In [4], the authors present an FPGA

implementation using Xilinx devices and calibration methodologies for a smart antenna digital beamforming consisting of eight channels and operating in L band (1.8 to 2GHz). A comparison of efficient broadband beamforming architectures is presented in [5]; however no comparison on hardware resource is reported. A low power ASIC implementation of 2Mbps antenna-rake combiner supporting both maximum ratio combining (MRC) and least mean square (LMS) filter is presented in [7] where a 107 MHz clock frequency and 550mW as highest rate power are achieved. In this paper, we implement both MRC and noise constrained LMS (NC-LMS) based beamforming techniques on FPGA, using rapid prototyping techniques (Matlab-Simulink). We evaluate the performance and hardware resource for both techniques.

This paper is organized as follows. A signal model is briefly described in Section 2. Beamforming techniques and performance evaluation using MRC and NC-LMS is presented in Section 3. The FPGA implementation and results of the beamforming techniques are described in Section 4. A conclusion is presented in Section 5.

2. SIGNAL MODEL

Consider a reverse link from K mobile stations to a base station with multiple antennas. Let T represents the symbol interval; $s_{i,t}[\eta] \in S$ (S is the symbol alphabet; $S = \{\pm 1\}$ for binary phase shift keying (BPSK) case and $S = \{\pm \sqrt{2} \pm j/\sqrt{2}\}$ for quadrature phase shift keying (QPSK) case) the η th symbol, and $d_{i,t}(r, \eta)$ the spreading waveform at the η th symbol of the i th transmission. The spreading waveform is written as

$$d_{i,t}(r, \eta) = \sum_{\tau=0}^{N-1} c_{i,t}[\tau, \eta] s(\tau - \tau_c) \quad \text{where } \tau_c \text{ is the chip}$$

interval; $N = T/\tau_c$ the processing gain; $c_{i,t}[\tau, \eta]$ the τ th element of the spreading sequence for the η th symbol of the i th transmission; and $s(\tau)$ is the chip waveform of unit energy. Assume that the base station is equipped with L antenna elements and $\mathbf{a}(\theta)$ denotes the array response vector to the signal with angle of arrival (AOA) θ . The channel vector $\mathbf{h}_{i,t}$ can be written as $\mathbf{h}_{i,t} \propto \mathbf{a}(\theta)$. For Rayleigh fading channels or would be a complex Gaussian random variable. For M multipaths, there would be M spatial

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G.,Saravanakumar, U.**



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DSP for Embedded and Real-Time Systems Robert Oshana, 2012-10-11 This Expert Guide gives you the techniques and technologies in digital signal processing DSP to optimally design and implement your embedded system Written by experts with a solutions focus this encyclopedic reference gives you an indispensable aid to tackling the day to day problems you face in using DSP to develop embedded systems With this book you will learn A range of development techniques for developing DSP code Valuable tips and tricks for optimizing DSP software for maximum performance The various options available for constructing DSP systems from numerous software components The tools available for developing DSP applications Numerous practical guidelines from experts with wide and lengthy experience of DSP application development Features Several areas of research being done in advanced DSP technology Industry case studies on DSP systems development DSP for Embedded and Real Time Systems is the reference for both the beginner and experienced covering most aspects of using today s DSP techniques and technologies for designing and implementing an optimal embedded system The only complete reference which explains all aspects of using DSP in embedded systems development making it a rich resource for every day use Covers all aspects of using today s DSP techniques and technologies for designing and implementing an optimal embedded system Enables the engineer to find solutions to all the problems they will face when using DSP

Design Methodologies and Tools for 5G Network Development and Application Suresh, P., Vairavel, G., Saravanakumar, U., 2020-12-25 The demand for mobile broadband will continue to increase in upcoming years largely driven by the need to deliver ultra high definition video 5G is not only evolutionary it also provides higher bandwidth and lower latency than the current generation technology More importantly 5G is revolutionary in that it is expected to enable fundamentally new applications with much more stringent requirements in latency and bandwidth 5G should help solve the last mile last kilometer problem and provide broadband access to the next billion users on earth at a much lower cost because of its use of new spectrum and its improvements in spectral efficiency 5G wireless access networks will need to combine several innovative aspects of decentralized and centralized allocation looking to maximize performance and minimize signaling load Research is currently conducted to understand the inspirations requirements and the promising technical options to boost and enrich activities in 5G Design Methodologies and Tools for 5G Network Development and Application presents the enhancement methods of 5G communication explores the methods for faster communication and provides a promising alternative solution that equips designers with the capability to produce high performance scalable and adoptable communication protocol This book provides complete design methodologies supporting tools for 5G communication and innovative works The design and evaluation of different proposed 5G structures signal integrity reliability low power techniques application mapping testing and future trends This book is ideal for researchers who are working in communication networks design and implementations industry personnel engineers practitioners academicians

and students who are interested in the evolution importance usage and technology adoption for 5G applications

Dissertation Abstracts International, 2007 **Index to IEEE Publications** Institute of Electrical and Electronics Engineers, 1996 Issues for 1973 cover the entire IEEE technical literature **FPGA Implementation of Beamforming and OFDMA for WiMAX System**, 2008 FPGA-based Implementation of a Digital Processor for an Instantaneous Frequency Measurement Receiver James M. Helton, 2007 Digital wideband receivers are essential elements used in electronic warfare EW applications Instantaneous Frequency Measurement IFM receivers are suitable for use in EW systems due to the ultrawide instantaneous radio frequency RF bandwidth fine frequency resolution and moderately high sensitivity and dynamic range Conventional IFM receivers use analog components such as power dividers crystal video detectors and hybrids This research presents the architecture and design implementation of a purely digital IFM receiver based on a patented algorithm courtesy of the United States Air Force The invention is capable of detecting a short wave pulse with 1 MHz error for every 100 nsec The benefits include a compact lightweight cost effective alternative to its analog counterpart The design was implemented and tested on Delphi's ADC3255 a PMC digitizer with Xilinx Virtex 4 FPGA The outputs were verified using Xilinx's ChipScope Pro *Design of Multi-Beam Hybrid Digital Beamforming Receivers* Suresh Madishetty, 2018 This thesis discusses a detailed study of the design and performance analysis of patch antenna arrays at different frequencies A linear hybrid array of 16 elements is built using patch antennas integrated with an RF front end using commercial off the shelf COTS components A well organized receiver chain that can work at a frequency in the range of 5.6 GHz is built using chip level components on a printed circuit board PCB This study mainly emphasizes the design and implementation of the comprehensive receiver beamforming systems using fast Fourier transform FFT algorithm and approximate discrete Fourier transform a DFT 1 A low complexity 32 beam multi beamformer at 5.8 GHz is designed built and implemented in real time using optimized digital FPGA cores as the digital back end which is collaborated work with Viduneth Ariyaratna The emanating beams were measured and verified using the FPGA based 32 element 5.8 GHz array setup which can generate 120 MHz bandwidth per channel The beams corresponding to the approximate DFT are in good agreement with the beams corresponding to the FFT with negligible error approximately less than 14 dB This setup can be used as a test bed to measure and evaluate various signal processing algorithms up to 32 linear array elements *FPGA Implementation for Complete Digital Quadrature AM Receiver* Yan Wan, 2004 **Wave-digital Filter Based Circuits for Beamforming and RF-FPGAs** Nilanka Thilina Rajapaksha, 2015 Selective spatial filtering of propagating plane waves based on their direction of arrival is termed as beamforming Ultra wideband beamforming is an essential signal processing step in many real world applications such as wireless communications radar radio astronomy and biomedical imaging The radio frequency field programmable gate array RF FPGA is a conceptual device envisioned by the Defense Advanced Research Projects Agency DARPA research community to bring reconfigurable implementation ability to the RF analog domain

Research on RF FPGA is important for the advancement of areas such as cognitive radio enhanced access to radio spectrum software defined radio and multi protocol communications This work explores analog and digital circuits based on the wave digital filter WDF realization structure that are suitable for digital analog beamforming applications and implementation of active filters on the conceptual RF FPGA device Digital infinite impulse response IIR 2 D and 3 D WDF beamforming architectures are capable of broadband beamforming with having low side lobe level array factors and lower arithmetic complexity Wave digital filter architectures having fan cone shape in the spatio temporal frequency domain are able to achieve approximately frequency independent beam patterns The IIR WDF architectures are proposed and implemented that are able to achieve a hexagonal cross section in the magnitude response which enables better packing density of sky area in certain applications The digital IIR WDF architectures are tested on chip using and FPGA based platform Resource consumption and operational frequency estimates from FPGA and standard cell application specific integrated circuit ASIC compilations are presented The superior sensitivity properties of the multi dimensional WDF architectures are demonstrated through simulation results A novel fixed point design method that eliminates overflow is introduced that can be utilized for all multi dimensional systolic array filter architectures Novel spatially discrete time continuous beamforming architectures based on the WDF realization are also introduced The same idea is proposed to be implemented for one dimensional filter realization which can be used as a re configurable filter realization platform for RF FPGA devices Preliminary Simulation Program with Integrated Circuit Emphasis SPICE level simulations have verified the feasibility of a modular analog building block that can be utilized to implement more complex circuits in a future effort

FPGA Implementation of Baseband Receiver for HIPERMAN System, 2007 **Integrated 60GHz RF Beamforming in CMOS** Yikun Yu, Peter G.M.

Baltus, Arthur H.M. van Roermund, 2011-01-06 Integrated 60GHz RF Beamforming in CMOS describes new concepts and design techniques that can be used for 60GHz phased array systems First general trends and challenges in low cost high data rate 60GHz wireless system are studied and the phased array technique is introduced to improve the system performance Second the system requirements of phase shifters are analyzed and different phased array architectures are compared Third the design and implementation of 60GHz passive and active phase shifters in a CMOS technology are presented Fourth the integration of 60GHz phase shifters with other key building blocks such as low noise amplifiers and power amplifiers are described in detail Finally this book describes the integration of a 60GHz CMOS amplifier and an antenna in a printed circuit board PCB package

FPGA Implementation of Rajendra Kumar's Adaptive Receiver for Higher Order Modulated Signal Over Fading Channel Falgun Bhagavatula, 2016 This project efficiently implements Rajendra Kumar Adaptive Receiver on FPGA with reduced number of gates Very High Speed Integrated Circuit Hardware Description Language VHDL codes and Xilinx ISE are used for replicating the adaptive receiver circuit on Nexys 3 Spartan 6 FPGA trainer board

Implementation of a WCDMA AAA Receiver on an FPGA Based Software Radio Platform Saju P. Kora, 2001

60 GHz 4-Element RF Beamforming Receiver Array Saihua Lin, 2011 Mm wave technology is attractive for non destructive high resolution imaging high data rate communication and automobile radar applications For example the large available bandwidth at the unlicensed 60 GHz band can potentially support up to 7 Gb/s in IEEE 802.11ad However one fundamental problem in mm wave technology is the high signal path loss Multiple antenna arrays can be exploited to compensate for this drawback Since CMOS technology has evolved to a stage where its performance is comparable to the traditional III V compound semiconductor counterpart low cost lower power design and integration of an mm wave wireless circuit in CMOS technology has become feasible In this work we first characterize the on chip passive elements and active elements in a 65 nm CMOS technology Slotted ground CPW and MSL lines are proposed which provide high Q 20 performance or flexible design capabilities Two low noise amplifiers LNA with and without cascode devices are implemented and compared The LNA without the cascode device turns out to be a better option It is shown that the cascode device will degrade noise figure bandwidth and linearity The noise figure without the cascode device is only 3.8 dB with 16.2 dB gain at 59 GHz 8.7 GHz bandwidth and 8.3 mA current consumption under the 1 V supply A 4 element RF beamforming receiver front end with four off chip antennas is implemented in 65 nm CMOS The front end is digitally controlled and based on the proposed phase oversampling vector modulation POVM method The receiver front end includes 4 LNAs 4 POVMs and power combining networks Four off chip antennas are wire bonded to the receiver Different substrate materials are experimented and compared for the antenna design including RO4003 FR4 and RT5880 materials Compared to state of the art work we achieve high phase resolution 3.5° very low NF 5.6 dB with high gain 18.5 dB for the beamformer at 56 GHz and demonstrate truly spatial power combining and beam steering by using antennas Compared with the conventional exhaustive lookup table method the proposed POVM uses a semi lookup table method It uses a very small lookup table consisting of only basic oversampling vectors and utilizes the linearity characteristics to adaptively select the weighting coefficients to compensate for the non idealities in circuits antenna array and interfaces

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