

# Solution Manual for CMOS Digital Integrated Circuits Analysis and Design 4th Edition Kang Leblebici Kim ISBN 0073380628 9780073380629

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## Exercise Problems

3.1 Consider a MOS system with the following parameters:

$$\begin{aligned} t_{ox} &= 1.6 \text{ nm} \\ \phi_c &= 1.04 \text{ V} \\ N_A &= 2.8 \times 10^{18} \text{ cm}^{-3} \\ Q_{ox} &= q \cdot 4 \times 10^{10} \text{ C/cm}^2 \end{aligned}$$

a. Determine the threshold voltage  $V_{T0}$  under zero bias at room temperature ( $T = 300 \text{ K}$ ).

Note that  $\epsilon_{ox} = 3.97 \epsilon_0$  and  $\epsilon_{si} = 11.7 \epsilon_0$ .

**SOLUTION:**

First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate:

$$\phi_{(substrate)} = \frac{kT}{q} \ln \frac{N_i}{N_A} = \frac{0.026 \text{ V}}{1} \ln \frac{1.5 \times 10^{10}}{2.8 \times 10^{18}} = -0.49 \text{ V}$$

The depletion region charge density at  $V_{SG} = 0$  is found as follows:

$$Q_{D0} = \sqrt{2 q N_A \epsilon_{si} | 2 \phi_{(substrate)} |} = \sqrt{2 \cdot 1.6 \times 10^{-19} \text{ C} \cdot (2.8 \times 10^{18} \text{ cm}^{-3}) \cdot 11.7 \cdot 8.85 \times 10^{-14} \text{ F/cm} \cdot 2 \cdot 0.49 \text{ V}} = 9.53 \times 10^{-7} \text{ C/cm}^2$$

The oxide-interface charge is:

$$Q_{ox} = q N_{ox} = 1.6 \times 10^{-19} \text{ C} \cdot 4 \times 10^{10} \text{ cm}^{-2} = 6.4 \times 10^{-9} \text{ C/cm}^2$$

The gate oxide capacitance per unit area is calculated using the dielectric constant of silicon dioxide and the oxide thickness  $t_{ox}$ :

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.97 \cdot 8.85 \times 10^{-14} \text{ F/cm}}{1.6 \times 10^{-7} \text{ cm}} = 2.2 \times 10^{-6} \text{ F/cm}^2$$

Now, we can combine all components and calculate the threshold voltage.

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## **Cmos Digital Integrated Circuits Kang Solution:**

Solution Manual to Accompany CMOS Digital Integrated Circuits : Analysis and Design, Second Edition Sung-Mo Kang, Yusuf Leblebici, 1999      **CMOS Digital Integrated Circuits** Sung-Mo Kang, Yusuf Leblebici, 1996 This text is the most comprehensive book on the market for CMOS circuits Aimed at junior senior courses offered in electrical engineering and computer science this book starts with CMOS processing and then covers MOS transition models basic CMOS gates dynamic circuits memory circuits BiCMOS circuits I O circuits VLSI design methodologies design for manufacturability and design for testability This text provides rigorous treatment of basic design concepts with detailed examples It addresses both design concepts and computer aided analysis for most of the circuit examples SPICE simulation results are provided for illustration

**Interconnect Technologies for Integrated Circuits and Flexible Electronics** Yash Agrawal, Kavicharan Mummaneni, P. Uma Sathyakam, 2023-09-21 This contributed book provides a thorough understanding of the basics along with detailed state of the art emerging interconnect technologies for integrated circuit design and flexible electronics It focuses on the investigation of advanced on chip interconnects which match the current as well as future technology requirements The contents focus on different aspects of interconnects such as material physical characteristics parasitic extraction design structure modeling machine learning and neural network based models for interconnects signaling schemes varying signal integrity performance analysis variability reliability aspects associated electronic design automation tools The book also explores interconnect technologies for flexible electronic systems It also highlights the integration of sensors with stretchable interconnects to demonstrate the concept of a stretchable sensing network for wearable and flexible applications This book is a useful guide for those working in academia and industry to understand the fundamentals and application of interconnect technologies      **Toward Quantum FinFET** Weihua Han, Zhiming M. Wang, 2013-11-23 This book reviews a range of quantum phenomena in novel nanoscale transistors called FinFETs including quantized conductance of 1D transport single electron effect tunneling transport etc The goal is to create a fundamental bridge between quantum FinFET and nanotechnology to stimulate readers interest in developing new types of semiconductor technology Although the rapid development of micro nano fabrication is driving the MOSFET downscaling trend that is evolving from planar channel to nonplanar FinFET silicon based CMOS technology is expected to face fundamental limits in the near future Therefore new types of nanoscale devices are being investigated aggressively to take advantage of the quantum effect in carrier transport The quantum confinement effect of FinFET at room temperatures was reported following the breakthrough to sub 10nm scale technology in silicon nanowires With chapters written by leading scientists throughout the world **Toward Quantum FinFET** provides a comprehensive introduction to the field as well as a platform for knowledge sharing and dissemination of the latest advances As a roadmap to guide further research in an area of increasing importance for the future development of materials science nanofabrication technology and nano electronic devices the book can be recommended for Physics

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**Reliability-aware Design of Integrated Circuits** Mohsen Raji,Behnam Ghavami,2022-11-16 This book covers the state of the art research in design of modern electronic systems used in safety critical applications such as medical devices aircraft flight control and automotive systems The authors discuss lifetime reliability of digital systems as well as an overview of the latest research in the field of reliability aware design of integrated circuits They address modeling approaches and techniques for evaluation and improvement of lifetime reliability for nano scale CMOS digital circuits as well as design algorithms that are the cornerstone of Computer Aided Design CAD of reliable VLSI circuits In addition to developing lifetime reliability analysis and techniques for clocked storage elements such as flip flops the authors also describe analysis and improvement strategies targeting commercial digital circuits **Field Effect Transistors** P. Suveetha Dhanaselvam,K.

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Jaewon Kim,University of Illinois at Urbana-Champaign. Department of Computer Science,1995 Abstract As the technology advances millions of transistors can be integrated on a small chip area With the trend the physical layout synthesis by human designers becomes costly and error prone due to the various design constraints Therefore the demands for intelligent tools have been increasing to create physical layouts for custom logic design We developed an automatic layout synthesis system for high performance full custom circuits In this thesis we introduce our synthesis system in conjunction with related problems and solutions Most of the problems in physical layout synthesis namely leaf cell construction partitioning placement

global routing detailed routing and transistor gate sizing are addressed in our synthesis system All necessary leaf cells are individually synthesized with customized transistor sizes before placement and tuned after detailed routing We developed various techniques for the leaf cell synthesis to match layout experts such as transistor folding transistor ordering contact placement and transistor sizing In partitioning and placement we concentrated our effort on data path circuits which is one of the currently popular topics For detailed routing a triple metal layer over the cell router has been developed for a popular platform Our synthesis system iteratively improves the layout until given requirements are satisfied We tested our system with various benchmark circuits to measure the performance Also a whole chip layout including bonding pads for DSP circuits has been synthesized with a hierarchical design scheme High Performance Dynamic Circuits Ge Yang,2003

*SOC Design Methodologies* Michel Robert,Bruno Rouzeyre,Christian Pigué,Marie-Lise Flottes,2013-03-15 The 11 th IFIP International Conference on Very Large Scale Integration in Montpellier France December 3 5 2001 was a great success The main focus was about IP Cores Circuits and System Designs 55 years ago in late 1947 the transistor was invented and everybody knows that it was by William Shockley John Bardeen and Walter H Brattain Bell Telephone Laboratories which received the Nobel Prize in Physics in 1956 Probably everybody thinks that it was recognized immediately as a major invention *Reliability Simulation of Digital CMOS VLSI Circuits* Eric Ricky Minami,1994 **Integrated Circuit and System Design** ,2003 **Proceedings of the ... International Conference on Microelectronics** ,2001 *Thermal and Power Integrity Analysis and Optimization for High Performance VLSI* Ting-Yuan Wang,2004 **CMOS Digital Integrated Circuits** Sung-Mo Kang,Yusuf Leblebici,2003 The fourth edition of CMOS Digital Integrated Circuits Analysis and Design continues the well established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design as well as addressing state of the art technology issues highlighted by the widespread use of nanometer scale CMOS technologies In this latest edition virtually all chapters have been re written the transistor model equations and device parameters have been revised to reflect the significant changes that must be taken into account for new technology generations and the material has been reinforced with up to date examples The broad ranging coverage of this textbook starts with the fundamentals of CMOS process technology and continues with MOS transistor models basic CMOS gates interconnect effects dynamic circuits memory circuits arithmetic building blocks clock and I O circuits low power design techniques design for manufacturability and design for testability **Progressive Random Access Scan** Dong Hyun Baik,2005 **Proceedings of the ... Midwest Symposium on Circuits and Systems** ,2000 **Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology** ,1997 *CMOS Digital Circuit Technology* Masakazu Shoji,1988 CMOS Digital Integrated Circuits Sung-Mo Kang,Yusuf Leblebici,Chulwoo Kim,2014-05 Offers comprehensive coverage of digital CMOS circuit design as well as addressing technology issues highlighted by the widespread use of nanometer scale CMOS technologies **30th Midwest Symposium on Circuits and Systems** Kamal Jabbour,1988

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