

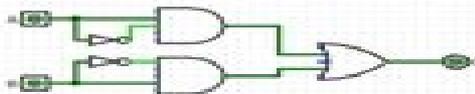
Computer Architecture 1 Final Exam

ELE319, Hanyang University, 2019 Spring.
ID: _____ Name: _____

Department: _____

The first two problems are mandatory. If you fail to answer the questions, you will not receive any credit.

- (5pt) Specify the 5-stage pipeline and explain what operation is performed at each stage.
- (5pt) Specify three hazards in processor pipelining and explain hardware and software approaches to solve the hazards.
- (5pt) Write the output value (C) for the given circuits if $A=1$ and $B=1$.



- (5pt) We construct a 2-bit multiplier using Mux as following. Two inputs are provided to a selector in Mux. For instance, $01 * 01 = 0001$ and $00 * 00 = 0000$ in the following figure. Fill the remained constant input values in the Mux to complete the multiplier. (1.5pt)



- (5pt) Similarly, we are constructing a divider using a ROM as following. In the example, if dividend is 5 and divisor is 2 then quotient is 2 and remainder is 1. Hence, $0x21$ is stored at address $0x52$. What value should be stored at address $0x53$ in the ROM to support the divider? (1.5pt)



- (5pt) What is the difference between latch and flip-flop? (5pt)
- (5pt) For the following arithmetic unit, we want to compute $A-B$ where 2's complement number is used. Determine proper values for $S1, S0, Cin$ to make $F = A-B$.



- (24pt) The following figure shows single cycle implementation for datapath and control path for MIPS architecture.



Fill 0, 1 or X(don't care) in the following table to implement for the architecture.

| Instruction | ALU Op | MEMRs of Reg | Reg Write | Mem Read | Mem Write | Branch |
|--------------------|--------|-----------------|-----------|----------|-----------|--------|
| R-type instruction | (1) | (2) | (3) | (4) | (5) | (6) |
| Load | (7) | (8) | (9) | (10) | (11) | (12) |
| Store | (13) | (14) | (15) | (16) | (17) | (18) |
| branch0 | (19) | (20) | (21) | (22) | (23) | (24) |

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