

## 4-bit Synchronous Counter (74LS161)

```
// 4-bit counter

module counter_4bit(clk, nclr, nload, ent, enp, rco, count, parallel_in) :

    input  clk ;
    input  nclr ;
    input  nload ;
    input  ent ;
    input  enp ;
    output rco ;
    output [3:0] count ;
    input  [3:0] parallel_in ;

    reg    [3:0] count ;
    reg    rco ;

    always @ (count or ent)
    if ((count == 15) && (ent == 1'b1))
        rco = 1'b1 ;
    else
        rco = 1'b0 ;

    always @ (posedge clk or negedge nclr)
    begin
        if (nclr == 1'b0)
            count <= 4'd0 ;
        else if (nload == 1'b0)
            count <= parallel_in ;
        else if ((ent == 1'b1) && (enp == 1'b1))
            count <= (count + 1) & 16 ;
    end
endmodule
```

# 4 Bit Counter Verilog Code Davefc

**Jin-Ying Zhang**



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