

FEATURES

- High speed (1.65 μ s) 12-bit ADC
- 4 simultaneously sampled inputs
- 4 track-and-hold amplifiers
- 0.35 μ s track-and-hold acquisition time
- 1.65 μ s conversion time per channel
- HW/SW select of channel sequence for conversion
- Single-supply operation
- Selection of input ranges
 - ± 10 V, ± 5 V for AD7864-1
 - ± 2.5 V for AD7864-3
 - 0 V to 2.5 V, 0 V to 5 V for AD7864-2
- High speed parallel interface that allows interfacing to 3 V processors
- Low power, 90 mW typical
- Power saving mode, 20 μ W typical
- Overshoot protection on analog inputs

APPLICATIONS

- AC motor control
- Uninterrupted power supplies
- Data acquisition systems
- Communications

GENERAL DESCRIPTION

The AD7864 is a high speed, low power, 4-channel, simultaneous sampling 12-bit analog-to-digital converter (ADC) that operates from a single 5 V supply. The part contains a 1.65 μ s successive approximation ADC, four track-and-hold amplifiers, a 2.5 V reference, an on-chip clock oscillator, signal conditioning circuitry, and a high speed parallel interface. The input signals on four channels sample simultaneously preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of ± 10 V, ± 5 V (AD7864-1), 0 V to +2.5 V, 0 V to +5 V (AD7864-2), and ± 2.5 V (AD7864-3).

Any subset of the four channels can be converted to maximize the throughput rate on the selected sequence. Select the channels to convert via hardware (channel select input pins) or software (programming the channel select register).

A single conversion start signal ($\overline{\text{CONVST}}$) simultaneously places all the track-and-holds into hold and initiates a conversion sequence for the selected channels. The $\overline{\text{EOC}}$ signal indicates the end of each individual conversion in the selected conversion sequence. The $\overline{\text{BUSY}}$ signal indicates the end of the conversion sequence.

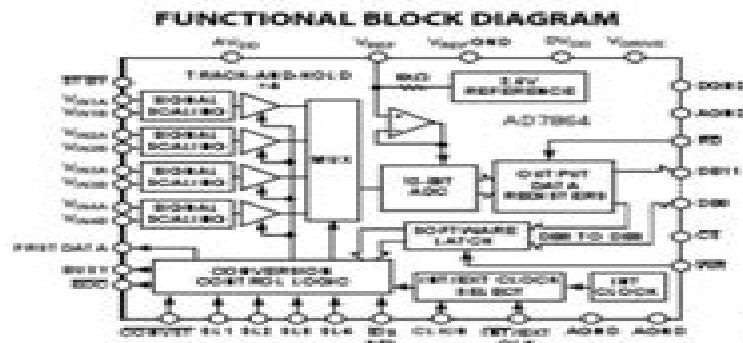


Figure 1.

Data is read from the part by a 12-bit parallel data bus using the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. Maximum throughput for a single channel is 500 kSPS. For all four channels, the maximum throughput is 130 kSPS for the read-during-conversion sequence operation. The throughput rate for the read-after-conversion sequence operation depends on the read cycle time of the processor. See the Timing and Control section. The AD7864 is available in a small (0.3 square inch area) 44-lead MQFP.

PRODUCT HIGHLIGHTS

1. Four track-and-hold amplifiers and a fast (1.65 μ s) ADC for simultaneous sampling and conversion of any subset of the four channels.
2. A single 5 V supply consuming only 90 mW typical, makes it ideal for low power and portable applications. See the Standby Mode Operation section.
3. High speed parallel interface for easy connection to microprocessors, microcontrollers, and digital signal processors.
4. Available in three versions with different analog input ranges. The AD7864-1 offers the standard industrial input ranges of ± 10 V and ± 5 V; the AD7864-3 offers the common signal processing input range of ± 2.5 V; the AD7864-2 can be used in unipolar, 0 V to 2.5 V and 0 V to 5 V, applications.
5. Features very tight aperture delay matching between the four input sample-and-hold amplifiers.

Rev. 0

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Table of Contents 4 Channel Simultaneous Sampling High Speed 12 Bit Adc

1. Understanding the eBook 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - The Rise of Digital Reading 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Advantages of eBooks Over Traditional Books
2. Identifying 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - User-Friendly Interface
4. Exploring eBook Recommendations from 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Personalized Recommendations
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc User Reviews and Ratings
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc and Bestseller Lists

5. Accessing 4 Channel Simultaneous Sampling High Speed 12 Bit Adc Free and Paid eBooks
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc Public Domain eBooks
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc eBook Subscription Services
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc Budget-Friendly Options
6. Navigating 4 Channel Simultaneous Sampling High Speed 12 Bit Adc eBook Formats
 - ePub, PDF, MOBI, and More
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc Compatibility with Devices
 - 4 Channel Simultaneous Sampling High Speed 12 Bit Adc Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Highlighting and Note-Taking 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Interactive Elements 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
8. Staying Engaged with 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
9. Balancing eBooks and Physical Books 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Setting Reading Goals 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Fact-Checking eBook Content of 4 Channel Simultaneous Sampling High Speed 12 Bit Adc
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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waterfall with cantilevered decks extending it into the surrounding forest it seems a part of its natural site

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pennsylvania about 70 miles 110 km southeast of pittsburgh in the united states 4 it is built partly over a waterfall on bear
run in the mill run section of stewart township fayette county pennsylvania

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from the waterfall running under the house fallingwater is located in bear run pennsylvania and was a weekend retreat for
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the house s daring construction over a waterfall was instrumental in reviving wright s career and it became one

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archive library of congress photo carol m highsmith perched above a mountain cataract on a rocky hillside deep in the
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