

Code No: 54023

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, July/August - 2021

STRUCTURED DIGITAL SYSTEM DESIGN

(Electronics and Instrumentation Engineering)

Time: 3 hours

Max. Marks: 75

Answer any five questions  
All questions carry equal marks

- 1.a) Design a BCD adder circuit.  
b) Design a 4-bit magnitude comparator circuit using above BCD adder. [7+8]
- 2.a) Explain the terms fan-out, fan-in.  
b) What is the worst case propagation delay of given network shown in figure 1?  $At_1 = 10$  nSec,  $At_2 = 20$  nSec,  $At_3 = 25$  nSec,  $At_4 = 10$  nSec. [7+8]



Figure: 1

- 3.a) Differentiate Moore machine from mealy machine.  
b) Convert an edge triggered D - Flip flop to an edge triggered JK flip flop. [7+8]
4. Using the state diagram make state assignment for the given state figure 2. [15]

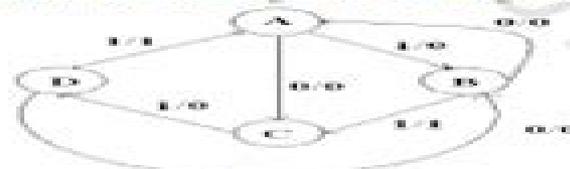


Figure: 2

5. Design a module - 6 Gray code counter. Make your code reflective with respect to the 2<sup>nd</sup> MSB. [15]
6. Design a controller that controls the drive circuit of stepper motor. Assume required control word format. [15]
- 7.a) Design a binary multiplier using parallel adder and shift register.  
b) Explain the concept of state assignment with examples. [9+6]
8. Write a short note on:  
a) FPLA architecture.  
b) Configurable memories. [7+8]

# Digital System Design Solved Question Papers

**Anthony S. Fauci**



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