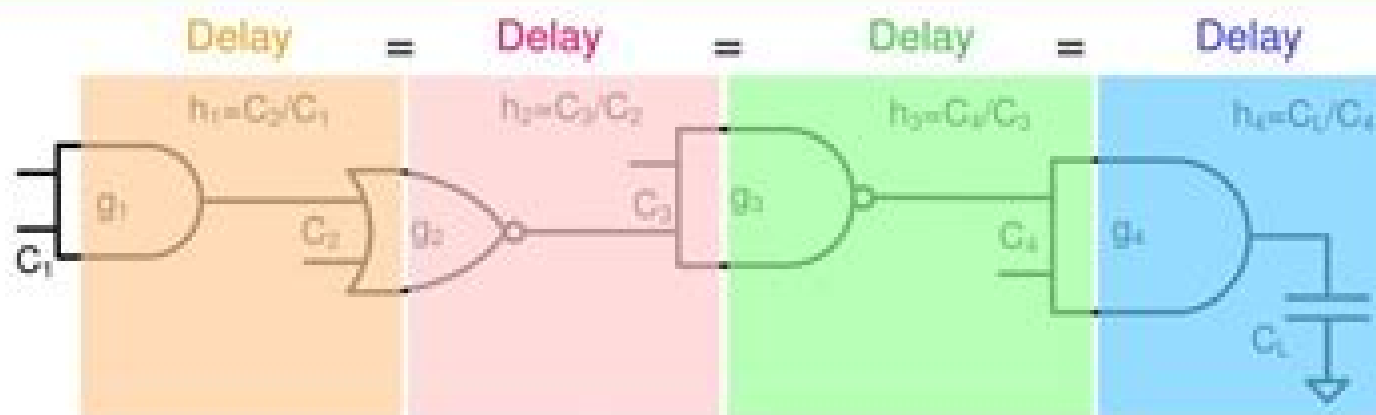


# Logical Effort (*only logic*)



*Delay model*

*Optimal sizing*

$$D_i = \tau \cdot g_i \cdot h_i + p_i$$

$$\text{Delay}_i = \text{Delay}_{i+1}$$

$\tau$  - delay of minimal inverter  $R_0 \cdot C_0$ , technology constant

$g_i$  - logical effort, gate type factor: e.g.  $g_{inv} = 1$

$h_i$  - electrical effort, load driving capability

$p_i$  - parasitic effort, due to output capacitance

$$g_i h_i = g_{i+1} h_{i+1}$$

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**Shyam Akashe, Khusbou Mishra**



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