

### FEATURES

Complete Multistage Log-Limiting IF Amplifier  
**100 dB Dynamic Range:**  $-78$  dBm to  $+22$  dBm (Re  $50 \Omega$ )  
**Stable RSSI Scaling Over Temperature and Supplies:**  
 20 mV/dB Slope,  $-95$  dBm Intercept  
 $\pm 0.4$  dB RSSI Linearity up to 200 MHz  
**Programmable Limiter Gain and Output Current**  
 Differential Outputs to 10 mA, 2.4 V p-p  
 Overall Gain 100 dB, Bandwidth 500 MHz  
 Constant Phase (Typical  $\pm 80$  ps Delay Skew)  
**Single Supply of +2.7 V to +6.5 V at 16 mA Typical**  
 Fully Differential Inputs,  $R_{in} = 1$  k $\Omega$ ,  $C_{in} = 2.5$  pF  
 500 ns Power-Up Time,  $<1 \mu\text{A}$  Sleep Current

### APPLICATIONS

Receivers for Frequency and Phase Modulation  
 Very Wide Range IF and RF Power Measurement  
 Receiver Signal Strength Indication (RSSI)  
 Low Cost Radar and Sonar Signal Processing  
 Instrumentation: Network and Spectrum Analyzers

### PRODUCT DESCRIPTION

The AD8309 is a complete IF limiting amplifier, providing both an accurate logarithmic (decibel) measure of the input signal (the RSSI function) over a dynamic range of 100 dB, and a programmable limiter output, useful from 5 MHz to 500 MHz.

It is easy to use, requiring few external components. A single supply voltage of +2.7 V to +6.5 V at 16 mA is needed, corresponding to a power consumption of under 50 mW at 3 V, plus the limiter bias current, determined by the application and typically 2 mA, providing a limiter gain of 100 dB when using 200  $\Omega$  loads. A CMOS-compatible control interface can enable the AD8309 within about 500 ns and disable it to a standby current of under 1  $\mu\text{A}$ .

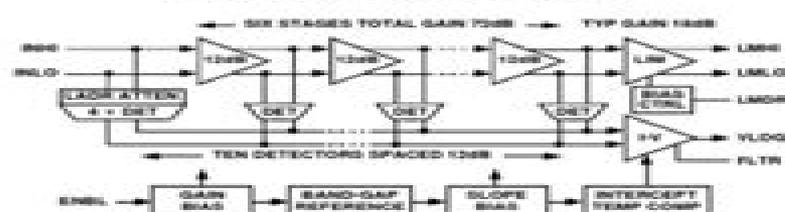
The six cascaded amplifier/limiter cells in the main path have a small signal gain of 12.04 dB ( $\approx 4$ ), with a  $-3$  dB bandwidth of 850 MHz, providing a total gain of 72 dB. The programmable output stage provides a further 18 dB of gain. The input is fully differential and presents a moderately high impedance (1 k $\Omega$  in parallel with 2.5 pF). The input-referred noise-spectral-density, when driven from a terminated 50  $\Omega$  source is 1.28 nV/ $\sqrt{\text{Hz}}$ , equivalent to a noise figure of 3 dB. The sensitivity of the AD8309 can be raised by using an input matching network.

Each of the main gain cells includes a full-wave detector. An additional four detectors, driven by a broadband attenuator, are used to extend the top end of the dynamic range by over 48 dB.

### REV. B

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### FUNCTIONAL BLOCK DIAGRAM



The overall dynamic range for this combination extends from  $-91$  dBV ( $-78$  dBm at the 50  $\Omega$  level) to a maximum permissible value of  $+9$  dBV, using a balanced drive of antiphase inputs each of 2 V in amplitude, which would correspond to a sine wave power of  $+22$  dBm if the differential input were terminated in 50  $\Omega$ . The slope of the RSSI output is closely controlled to 20 mV/dB, while the intercept is set to  $-108$  dBV ( $-95$  dBm re 50  $\Omega$ ). These scaling parameters are determined by a band-gap voltage reference and are substantially independent of temperature and supply. The logarithmic law conformance is typically within  $\pm 0.4$  dB over the central 80 dB of this range at any frequency between 10 MHz and 200 MHz, and is degraded only slightly at 500 MHz.

The RSSI response time is nominally 67 ns (10%–90%). The averaging time may be increased without limit by the addition of an external capacitor. The full output of 2.34 V at the maximum input of  $+9$  dBV can drive any resistive load down to 50  $\Omega$  and this interface remains stable with any value of capacitance on the output.

The AD8309 is fabricated on an advanced complementary bipolar process using silicon-on-insulator isolation techniques and is available in the industrial temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ , in a 16-lead TSSOP package.

# A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz

**CH Cherryholmes**



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## **Table of Contents A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz**

1. Understanding the eBook A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - The Rise of Digital Reading A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Advantages of eBooks Over Traditional Books
2. Identifying A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - User-Friendly Interface
4. Exploring eBook Recommendations from A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Personalized Recommendations
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz User Reviews and Ratings
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz and Bestseller Lists
5. Accessing A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz Free and Paid eBooks
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz Public Domain eBooks
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz eBook Subscription Services

- A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz Budget-Friendly Options
- 6. Navigating A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz eBook Formats
  - ePub, PDF, MOBI, and More
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz Compatibility with Devices
  - A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz Enhanced eBook Features
- 7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Highlighting and Note-Taking A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Interactive Elements A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
- 8. Staying Engaged with A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
- 9. Balancing eBooks and Physical Books A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
- 10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
- 11. Cultivating a Reading Routine A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Setting Reading Goals A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Fact-Checking eBook Content of A Logarithmic Amplifier With Limiter Output 5 Mhz 500 Mhz
  - Distinguishing Credible Sources
- 13. Promoting Lifelong Learning
  - Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
- 14. Embracing eBook Trends

- Integration of Multimedia Elements
- Interactive and Gamified eBooks

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