

Digital Electronics

CHARACTERISTICS OF LOGIC FAMILY



PROPAGATION DELAY (t_{pd})

Measured in nano seconds (ns)

Time taken for signal to change from ON to OFF. Time is more due to storage time.

Time taken for signal to change from OFF to ON (t_{rise}) > t_{fall} due to storage time or saturation delay.



Due to the propagation delay in the gates, the output response is not exactly identical to the input signal when the input is applied.



$$t_{pd} = \frac{t_{rise} + t_{fall}}{2}$$

In reality, sudden changes (transitions from 0 to 1 or vice versa) doesn't happen instantaneously. Sometimes it spent some time (rising and falling) before vice versa.

All logic family is the fastest among all.

POWER DISSIPATION

Power dissipation is power dissipated by a logic gate.

Measured in milliwatts (mW)

Mathematically

$$P_{diss} = V_{cc} \times I_{c(avg)}$$

$$I_{c(avg)} = \frac{I_c(ON) + I_c(OFF)}{2}$$

I_{c(OFF)} = I_{c(LEAK)}

I_{c(ON)} = (cut off current)

CMOS logic family has lowest power dissipation.

Ideally should be zero, but practically low current.



$$V_{cc} - V_{ce(sat)} = I_{c(sat)} R_L$$

$$I_{c(sat)} \approx \frac{V_{cc}}{R_L}$$

FIGURE OF MERIT

Mathematically

$$F.O.M = t_{pd} \times P_{diss}$$

$$= ns \times mW$$

$$= pJ \text{ (Picjoules)}$$

$$CMOS \approx 0.1 pJ \text{ (Picjoules)}$$

Best F.O.M is for CMOS logic family among all logic families. CMOS has F.O.M. in range of 0.1 pJ to 0.7 pJ.

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L Reisser



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