Active Matrix Driving and Circuit Simulation

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1. Introduction

This chapter explains the principle of active matrix driving which is the most popular driving method used in current liquid crystal displays (LCDs). It then discusses issues that designers must overcome to avoid the malfunctioning and introduces a liquid crystal model for conducting circuit simulations to optimize the circuit parameters efficiently.

1.1 Equivalent circuit of a pixel in LCDs

The equivalent circuit of a pixel operated by active matrix driving is shown in Fig. 1.
Data lines are connected to a data driver for generating the signal pulses for the picture data. Scan lines are connected to a scan driver for generating the scan pulses which enable the addressing driving. Vsig and Vg are applied to the data lines and scan lines, respectively. The thin film transistor (TFT) has three terminals of MOS transistors, and each terminal gate, drain, and source is connected to a scan line, a data line, and a pixel electrode, respectively. Cgs means the parasitic capacitance between the gate and source terminal in the TFT. Liquid crystal is injected into the gap between the pixel electrode and the counter backplane electrode, and it forms a liquid crystal cell capacitance (Clc). Clc is a variable capacitor that changes value according to the applied voltage between the pixel electrode and a counter backplane electrode. The voltage of the pixel electrode and counter backplane electrode are denoted by Vpix and Vcom, respectively. The storage capacitor is denoted Csc, and it is connected in parallel to Clc. Its function is to hold charges on a pixel electrode while the TFT is switched off.

1.2 Timing chart for each signal pulse

Fig. 2 shows the wave forms applied to each bus line and electrode. The period during which the pixel electrode voltage (Vpix) is higher than the counter electrode voltage (Vcom) is called the "plus frame" (Fig.2 (a)), whereas the period during which Vpix is lower than Vcom is called the "minus frame" (Fig.2 (b)). The plus and minus frames are switched every frame period (Tf).
When the voltage of the gate terminal connecting to the scan line rise to a high level, the resistance between the drain and source terminals becomes very low (Ron). As a result, electrical charges flow into the pixel electrode from the data line till the voltage of the pixel electrode achieves the voltage of the data line during the writing time (Tw). This process is called the "Charge Process". When the voltage of the scan line starts to drop, the pixel electrode voltage shows a negative shift ΔVfd because of the coupling with the gate terminal

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