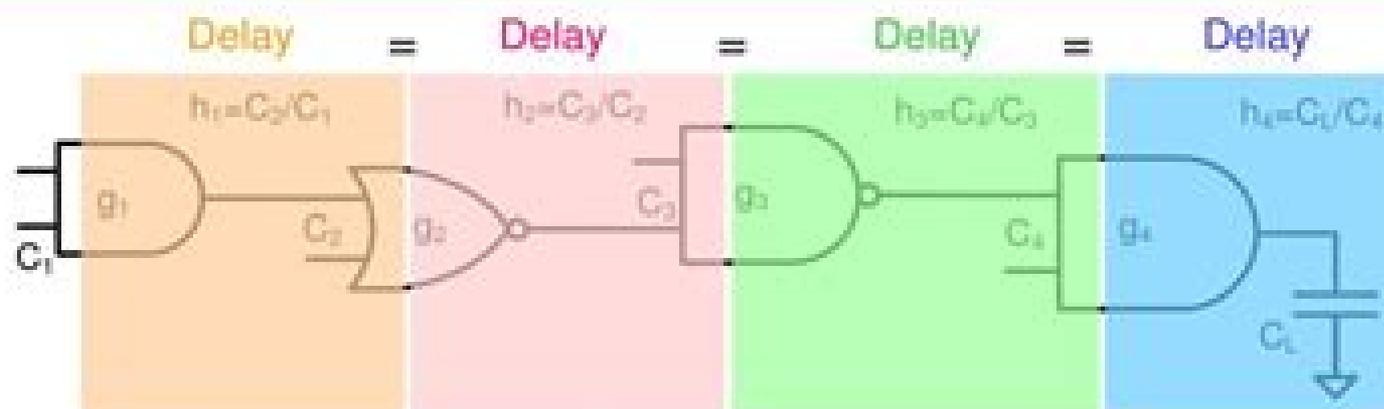


# Logical Effort (*only logic*)



*Delay model*

*Optimal sizing*

$$D_i = \tau \cdot g_i \cdot h_i + p_i$$

$$\text{Delay}_i = \text{Delay}_{i+1}$$

$\tau$  - delay of minimal inverter  $R_0 \cdot C_0$ , technology constant

$g_i$  - logical effort, gate type factor: e.g.  $g_{inv} = 1$

$h_i$  - electrical effort, load driving capability

$p_i$  - parasitic effort, due to output capacitance

$$g_i h_i = g_{i+1} h_{i+1}$$

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Logical Effort Ivan Sutherland, Robert F. Sproull, David Harris, 1999 Designers of high speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets Logical Effort Designing Fast CMOS Circuits makes high speed design easier and more methodical providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology capacitance and gate sizes The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull logical effort will change the way you approach design challenges This book begins by equipping you with a sound understanding of the method s essential procedures and concepts so you can start using it immediately Later chapters explore the theory and finer points of the method and detail its specialized applications Features Explains the method and how to apply it in two practically focused chapters Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions Offers easy ways to choose the fastest circuit from among an array of potential circuit designs Reduces the time spent on tweaking and simulations so you can rapidly settle on a good design Offers in depth coverage of specialized areas of application for logical effort skewed or unbalanced gates other circuit families including pseudo NMOS and domino wide structures such as decoders and irregularly forking circuits Presents a complete derivation of the method so you see how and why it works

**CMOS Processors and Memories** Krzysztof Iniewski, 2010-08-09 CMOS Processors and Memories addresses the state of the art in integrated circuit design in the context of emerging computing systems New design opportunities in memories and processor are discussed Emerging materials that can take system performance beyond standard CMOS like carbon nanotubes graphene ferroelectrics and tunnel junctions are explored CMOS Processors and Memories is divided into two parts processors and memories In the first part we start with high performance low power processor design followed by a chapter on multi core processing They both represent state of the art concepts in current computing industry The third chapter deals with asynchronous design that still carries lots of promise for future computing needs At the end we present a hardware design space exploration methodology for implementing and analyzing the hardware for the Bayesian inference framework This particular methodology involves analyzing the computational cost and exploring candidate hardware components proposing various custom architectures using both traditional CMOS and hybrid nanotechnology CMOL The first part concludes with hybrid CMOS Nano architectures The second memory part covers state of the art SRAM DRAM and flash memories as well as emerging device concepts Semiconductor memory is a good example of the full custom design that applies various analog and logic circuits to utilize the memory cell s device physics Critical physical effects that include tunneling hot electron injection charge trapping Flash memory are discussed in detail Emerging memories like FRAM PRAM and ReRAM that depend on magnetization electron spin alignment ferroelectric effect built in potential well quantum effects and thermal melting are also described CMOS Processors and Memories is a must for anyone serious about circuit design for



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**CMOS** R. Jacob Baker,2008 This edition provides an important contemporary view of a wide range of analog digital circuit blocks the BSIM model data converter architectures and more The authors develop design techniques for both long and short channel CMOS technologies and then compare the two

**Digital CMOS Circuit Design** Silvia Annaratone,2012-12-06

**Ultra High-Speed CMOS Circuits** Sam Gharavi,Babak Heydari,2011-09-25 The book covers the CMOS based millimeter wave circuits and devices and presents methods and design techniques to use CMOS technology for circuits operating beyond 100 GHz Coverage includes a detailed description of both active and passive devices including modeling techniques and performance optimization Various mm wave circuit blocks are discussed emphasizing their design distinctions from low frequency design methodologies This book also covers a device oriented circuit design technique that is essential for ultra high speed circuits and gives some examples of device circuit co design that can be used for mm wave technology

**CMOS VLSI Design** Neil H. E. Weste,David F. Harris,2005 Details techniques for the design of complex and high performance CMOS Systems on Chip This edition explains practices of chip design covering transistor operation CMOS gate design fabrication and layout at level accessible to anyone with an elementary knowledge of digital electronics

**High Speed CMOS Design Styles** Kerry Bernstein,K.M. Carrig,Christopher M. Durham,Patrick R. Hansen,David Hogenmiller,Edward J. Nowak,Norman J. Rohrer,2012-12-06 High Speed CMOS Design Styles is written for the graduate level student or practicing engineer who is primarily interested in circuit design It is intended to provide practical reference or horse sense to mechanisms typically described with a more academic slant This book is organized so that it can be used as a textbook or as a reference book High Speed CMOS Design Styles provides a survey of design styles in use in industry specifically in the high speed microprocessor design community Logic circuit

structures I/O and interface clocking and timing schemes are reviewed and described Characteristics sensitivities and idiosyncrasies of each are highlighted High Speed CMOS Design Styles also pulls together and explains contributors to performance variability that are associated with process applications conditions and design Rules of thumb and practical references are offered Each of the general circuit families is then analyzed for its sensitivity and response to this variability High Speed CMOS Design Styles is an excellent source of ideas and a compilation of observations that highlight how different approaches trade off critical parameters in design and process space

**Principles of CMOS VLSI Design** Neil H. E. Weste, Kamran Eshraghian, 1993 With this revision Weste conveys an understanding of CMOS technology circuit design layout and system design sufficient to the designer The book deals with the technology down to the layout level of detail thereby providing a bridge from a circuit to a form that may be fabricated

Modern CMOS Circuits Manual R. M. Marston, 1996 This Circuits Manual examines operating principles and practical applications of modern medium speed and fast CMOS digital ICs 470 carefully selected circuits diagrams graphs and tables are supported by the informative how to text and by detailed descriptions of more than 120 modern CMOS ICs and their practical applications Although ideal for practical design engineers and technicians this book will doubtless also be of great interest to hobbyists and students of electronics Using clear and comprehensive language each chapter begins with an explanation of the basic principles of the subject followed by the presentation of circuits and useful data The first chapter describes and explains digital IC basics CMOS and TTL principles the various CMOS sub families and CMOS basic usage rules Chapter 2 gives a practical introduction to CMOS basics via the 4007UB IC which can be used in both digital and linear applications Chapter 3 deals with modern logic circuitry and Chapter 4 with CMOS bilateral switches and data selectors The next six chapters progress through waveform generator circuitry clocked flip flop and counter circuits ICs special counter dividers data latches registers comparators and code converters Chapter 11 focuses on specialised types of IC such as multiplexers and decoders while the final chapter presents a miscellaneous collection of useful CMOS circuits

**Low Power High Speed CMOS Multiplexer Design** Shyam Akashe, Khusbou Mishra, 2015 This book proposes the reversible logic Multiplexer and also demarcates between reversible and irreversible logic Multiplexers For power reduction in future computing technologies reversible logic is a very productive approach of logic synthesis The purpose of this book is to reduce power and area of 2:1 MUX 4:1 MUX and reversible logic while maintaining the viable performance The diverse configurations are designed using different topologies of 2:1 MUX and 4:1 MUX such as CMOS based MUX transmission gate and pass transistor The editors propose a new application of GDI Gate Diffusion Input circuits to Reversible logic multiplexer with its Garbage input and output The novel proposed design technique will consume less power than the other conventional gate Reversible logic circuit has displayed less power dissipation in recent years Additionally this GDI cell technique decreases the power of the circuit delay Power Delay Product PDP and it also compacts the frequency The device scaling is partial as the power dissipation is more

optimized in terms of delay frequency jitter bandwidth power supply frequency and duty cycle of the signal and also establishes the noise of the circuit In the reversible logic design the GDI is efficient in lower delay low power and low leakage current

**Testing and Reliable Design of CMOS Circuits** Niraj K. Jha, Sandip Kundu, 2012-12-06 In the last few years CMOS technology has become increasingly dominant for realizing Very Large Scale Integrated VLSI circuits The popularity of this technology is due to its high density and low power requirement The ability to realize very complex circuits on a single chip has brought about a revolution in the world of electronics and computers However the rapid advancements in this area pose many new problems in the area of testing Testing has become a very time consuming process In order to ease the burden of testing many schemes for designing the circuit for improved testability have been presented These design for testability techniques have begun to catch the attention of chip manufacturers The trend is towards placing increased emphasis on these techniques Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults In order to take care of this problem we need to build fault tolerant systems The area of fault tolerant computing has steadily gained in importance Today many universities offer courses in the areas of digital system testing and fault tolerant computing Due to the importance of CMOS technology a significant portion of these courses may be devoted to CMOS testing This book has been written as a reference text for such courses offered at the senior or graduate level Familiarity with logic design and switching theory is assumed The book should also prove to be useful to professionals working in the semiconductor industry

*Cmos Logic Circuit Design* Uyemura, 2005-01-01

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